		22	With specified semiconductor
When placing a mandatory classification in			materials
Class 257, a cross-reference classifica-		23	Current flow across well
tion is normally made in at least one of		24	Field effect device
the appe	ended E-subclasses.	25	Employing resonant tunneling
		26	Ballistic transport device
		27	Field effect transistor
		28	
_		∠0	.Non-heterojunction superlattice
1	BULK EFFECT DEVICE		(e.g., doping superlattice or
2	.Bulk effect switching in		alternating metal and
	amorphous material		insulator layers)
3	With means to localize region	29	.Ballistic transport device
	of conduction (e.g., "pore"		(e.g., hot electron
	structure)		transistor)
4	With specified electrode	30	.Tunneling through region of
	composition or configuration		reduced conductivity
5	In array	31	Josephson
6	.Intervalley transfer (e.g., Gunn	32	Particular electrode material
Ü	effect)	33	High temperature (i.e., >30o
7	,		Kelvin)
/	In monolithic integrated	34	Weak link (e.g., narrowed
0	circuit	31	portion of superconductive
8	Three or more terminal device		line)
9	THIN ACTIVE PHYSICAL LAYER WHICH	35	Particular barrier material
	IS (1) AN ACTIVE POTENTIAL		
	WELL LAYER THIN ENOUGH TO	36	With additional electrode to
	ESTABLISH DISCRETE QUANTUM		control conductive state of
	ENERGY LEVELS OR (2) AN ACTIVE		Josephson junction
	BARRIER LAYER THIN ENOUGH TO	37	At least one electrode layer of
	PERMIT QUANTUM MECHANICAL		semiconductor material
	TUNNELING OR (3) AN ACTIVE	38	Three or more electrode device
	LAYER THIN ENOUGH TO PERMIT	39	Three or more electrode device
	CARRIER TRANSMISSION WITH	40	ORGANIC SEMICONDUCTOR MATERIAL
	SUBSTANTIALLY NO SCATTERING	41	POINT CONTACT DEVICE
	(E.G., SUPERLATTICE QUANTUM	42	SEMICONDUCTOR IS SELENIUM OR
	WELL, OR BALLISTIC TRANSPORT		TELLURIUM IN ELEMENTAL FORM
	DEVICE)	43	SEMICONDUCTOR IS AN OXIDE OF A
10	.Low workfunction layer for	13	METAL (E.G., CUO, ZNO) OR
	electron emission (e.g.,		COPPER SULFIDE
	photocathode electron emissive	4.4	****
	layer)	44	WITH METAL CONTACT ALLOYED TO
11	Combined with a heterojunction		ELEMENTAL SEMICONDUCTOR TYPE
	involving a III-V compound		PN JUNCTION IN NONREGENERATIVE
12	.Heterojunction		STRUCTURE
13		45	.Elongated alloyed region (e.g.,
	Incoherent light emitter		thermal gradient zone melting,
14	Quantum well		TGZM)
15	Superlattice	46	.In pn junction tunnel diode
16	Of amorphous semiconductor		(Esaki diode)
	material	47	.In bipolar transistor structure
17	With particular barrier	48	TEST OR CALIBRATION STRUCTURE
	dimension	49	NON-SINGLE CRYSTAL, OR
18	Strained layer superlattice		RECRYSTALLIZED, SEMICONDUCTOR
19	Si x Ge 1-x		MATERIAL FORMS PART OF ACTIVE
20	Field effect device		JUNCTION (INCLUDING FIELD-
21	Light responsive structure		INDUCED ACTIVE JUNCTION)
	. 5 :		

257 - 2 CLASS 257 ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID-STATE DIODES)

50	<pre>.Non-single crystal, or recrystallized, active junction adapted to be electrically shorted (e.g., "anti-fuse" element)</pre>	65	.Non-single crystal, or recrystallized, material containing non-dopant additive, or alloy of semiconductor materials (e.g.,
51	.Non-single crystal, or recrystallized, material forms active junction with single		Ge x Si 1- x, polycrystalline silicon with dangling bond modifier)
	<pre>crystal material (e.g., monocrystal to polycrystal pn junction or heterojunction)</pre>	66	<pre>.Field effect device in non- single crystal, or recrystallized, Semiconductor</pre>
52	.Amorphous semiconductor material		material
53	Responsive to nonelectrical	67	In combination with device
54	external signals (e.g., light)With Schottky barrier to		<pre>formed in single crystal semiconductor material (e.g., stacked FETs)</pre>
	amorphous material	68	,
55	Amorphous semiconductor is alloy or contains material to change band gap (e.g., Si x Ge	00	Capacitor element in single crystal semiconductor (e.g., DRAM)
	1-x , SiN y)	69	Field effect transistor in
56	With impurity other than	0,5	single crystal material,
50	hydrogen to passivate dangling bonds (e.g., halide)		complementary to that in non- single crystal, or
57	Field effect device in		recrystallized, material
37	amorphous semiconductor		(e.g., CMOS)
	material	70	Recrystallized semiconductor
58	With impurity other than		material
30	hydrogen to passivate dangling	71	In combination with capacitor
	bonds (e.g., halide)	. –	element (e.g., DRAM)
59	In array having structure for	72	In array having structure for
37	use as imager or display, or		use as imager or display, or
	with transparent electrode		with transparent electrode
60	With field electrode under or	73	.Schottky barrier to
	on a side edge of amorphous		polycrystalline semiconductor
	semiconductor material (e.g.,		material
	vertical current path)	74	.Plural recrystallized
61	With heavily doped regions		semiconductor layers (e.g.,
	contacting amorphous		"3-dimensional integrated
	semiconductor material (e.g.,		circuit")
	heavily doped source and	75	.Recrystallized semiconductor
	drain)		material
62	With impurity other than	76	SPECIFIED WIDE BAND GAP (1.5EV)
	hydrogen to passivate dangling bonds (e.g., halide)		SEMICONDUCTOR MATERIAL OTHER THAN GAASP OR GAALAS
63	Amorphous semiconductor is	77	.Diamond or silicon carbide
	alloy or contains material to	78	.II-VI compound
	change band gap (e.g., Si x Ge	79	INCOHERENT LIGHT EMITTER
	1-x , SiN y)		STRUCTURE
64	.Non-single crystal, or	80	.In combination with or also
	recrystallized, material with		constituting light responsive
	specified crystal structure		device
	<pre>(e.g., specified crystal size or orientation)</pre>	81	With specific housing or contact structure

82	Discrete light emitting and light responsive devices	106	.Reverse bias tunneling structure (e.g., "backward" diode, true
83	Light coupled transistor structure	107	Zener diode) REGENERATIVE TYPE SWITCHING
84	Combined in integrated structure	107	DEVICE (E.G., SCR, COMFET, THYRISTOR)
85	With heterojunction	108	.Controlled by nonelectrical,
86	.Active layer of indirect band gap semiconductor		<pre>nonoptical external signal (e.g., magnetic field,</pre>
87	With means to facilitate		pressure, thermal)
	<pre>electron-hole recombination (e.g., isoelectronic traps such as nitrogen in GaP)</pre>	109	<pre>.Having only two terminals and no control electrode (gate), e.g., Shockley diode</pre>
88	<pre>.Plural light emitting devices (e.g., matrix, 7-segment array)</pre>	110	<pre>More than four semiconductor layers of alternating conductivity types (e.g.,</pre>
89	Multi-color emission		pnpnpn structure, 5 layer
90	With heterojunction		bidirectional diacs, etc.)
91	With shaped contacts or opaque masking	111	Triggered by V BO overvoltage means
92	Alphanumeric segmented array	112	With highly-doped breakdown
93	With electrical isolation means		diode trigger
	in integrated circuit	113	.With light activation
	structure	114	With separate light detector
94	.With heterojunction		integrated on chip with
95	With contoured external surface		regenerative switching device
	<pre>(e.g., dome shape to facilitate light emission)</pre>	115	With electrical trigger signal amplification means (e.g.,
96	Plural heterojunctions in same device		<pre>amplified gate, "pilot thyristor", etc.)</pre>
97	More than two heterojunctions	116	With light conductor means
98	in same device .With reflector, opaque mask, or		(e.g., light fiber or light pipe) integral with device or
	optical element (e.g., lens,	110	device enclosure or package
	optical fiber, index of refraction matching layer,	117	In groove or with thinned semiconductor portion
	luminescent material layer,	118	With groove or thinned light
	filter) integral with device	110	sensitive portion
	or device enclosure or package	119	.Bidirectional rectifier with
99	.With housing or contact structure		<pre>control electrode (gate) (e.g., Triac)</pre>
100	.Encapsulated	120	Six or more semiconductor
101	.With particular dopant concentration or concentration		<pre>layers of alternating conductivity types (e.g., npnpnpn structure)</pre>
	profile (e.g., graded	121	With diode or transistor in
102	<pre>junction) .With particular dopant material</pre>	•	reverse path
102		122	Lateral
103	(e.g., zinc as dopant in GaAs) .With particular semiconductor	123	With trigger signal
	material		amplification (e.g., amplified
104	TUNNELING PN JUNCTION (E.G., ESAKI DIODE) DEVICE	124	gate)Combined with field effect
105	.In three or more terminal device	125	transistor structureControllable emitter shunting

257 - 4 CLASS 257 ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID-STATE DIODES)

126	With means to separate a device into sections having different	152	Cathode emitter or cathode electrode feature
127	conductive polarityGuard ring or groove	153	Gate region or electrode feature
128	Having overlapping sections of different conductive polarity	154	.With resistive region connecting separate sections of device
129	With means to increase reverse breakdown voltage	155	.With switching speed enhancement means (e.g., Schottky contact)
130	Switching speed enhancement means	156	Having deep level dopants or recombination centers
131	Recombination centers or deep level dopants	157	.With integrated trigger signal amplification means (e.g.,
132	.Five or more layer unidirectional structure		<pre>amplified gate, "pilot thyristor", etc.)</pre>
133	.Combined with field effect transistor	158	Three or more amplification stages
134	J-FET (junction field effect	159	Transistor as amplifier
135	transistor)Vertical (i.e., where the	160	With distributed amplified current
133	source is located above the	161	With a turn-off diode
	drain or vice versa)	162	
126	•		.Lateral structure
136	Enhancement mode (e.g., so-	163	.Emitter region feature
	called SITs)	164	Multi-emitter region (e.g.,
137	Having controllable emitter shunt		<pre>emitter geometry or emitter ballast resistor)</pre>
138	Having gate turn off (GTO)	165	Laterally symmetric regions
	feature	166	Radially symmetric regions
139	With extended latchup current level (e.g., COMFET device)	167	.Having at least four external electrodes
140	Combined with other solid-	168	.With means to increase breakdown
	state active device in		voltage
	integrated structure	169	High resistivity base layer
141	Lateral structure, i.e.,	170	Surface feature (e.g., guard
111	current flow parallel to main device surface	171	ring, groove, mesa, etc.)
142	Having impurity doping for		Edge feature (e.g., beveled edge)
1.40	gain reduction	172	.With means to lower "ON" voltage
143	Having anode shunt means		drop
144	Cathode emitter or cathode electrode feature	173	<pre>.Device protection (e.g., from overvoltage)</pre>
145	Low impedance channel contact extends below surface	174	<pre>Rate of rise of current (e.g., dI/dt)</pre>
146	.Combined with other solid-state active device in integrated structure	175	<pre>.With means to control triggering (e.g., gate electrode configuration, Zener diode</pre>
147	.With extended latchup current level (e.g., gate turn off "GTO" device)		firing, dV/Dt control, transient control by ferrite bead, etc.)
148	Having impurity doping for gain reduction	176	Located in an emitter-gate region
149	Having anode shunt means	177	.With housing or external
150	With specified housing or external terminal		electrode
151	External gate terminal structure or composition		

178	With means to avoid stress between electrode and active device (e.g., thermal expansion matching of electrode to semiconductor)	200	.Heterojunction formed between semiconductor materials which differ in that they belong to different periodic table groups (e.g., Ge (group IV) -
179 180	With malleable electrode (e.g., silver electrode layer)Stud mount		GaAs (group III-V) or InP (group III-V) - CdTe (group II-VI))
		201	
181	With large area flexible electrodes in press contact with opposite sides of active	201	.Between different group IV-VI or II-VI or III-V compounds other than GaAs/GaAlAs
	semiconductor chip and	202	GATE ARRAYS
	-	203	.With particular chip input/
	<pre>surrounded by an insulating element, (e.g., ring)</pre>	203	output means
182	With lead feedthrough means on	204	.Having specific type of active
	side of housing		device (e.g., CMOS)
183	HETEROJUNCTION DEVICE	205	With bipolar transistors or
183.1	.Charge transfer device		with FETs of only one channel
184	.Light responsive structure		conductivity type (e.g.,
185	Staircase (including graded		enhancement-depletion FETs)
	composition) device	206	Particular layout of
186	Avalanche photodetection		complementary FETs with regard
	structure	000	to each other
187	Having transistor structure	207	.With particular power supply
188	Having narrow energy band gap		distribution means
	<pre>(<<1eV) layer (e.g., PbSnTe, HgCdTe, etc.)</pre>	208	.With particular signal path connections
189	Layer is a group III-V	209	Programmable signal paths
109		_0,	(e.g., with fuse elements,
100	semiconductor compound		laser programmable, etc)
190	.With lattice constant mismatch	210	
	(e.g., with buffer layer to		With wiring channel area
	accommodate mismatch)	211	Multi-level metallization
191	.Having graded composition	212	CONDUCTIVITY MODULATION DEVICE
192	.Field effect transistor		(E.G., UNIJUNCTION TRANSISTOR,
194	Doping on side of		DOUBLE-BASE DIODE,
	heterojunction with lower		CONDUCTIVITY-MODULATED
	carrier affinity (e.g., high		TRANSISTOR)
	electron mobility transistor	213	FIELD EFFECT DEVICE
	(HEMT))	214	.Charge injection device
195	Combined with diverse type	215	.Charge transfer device
100	device	216	Majority signal carrier (e.g.,
106		210	buried or bulk channel, or
196	.Both semiconductors of the		•
	heterojunction are the same	015	peristaltic)
	conductivity type (i.e.,	217	Having a conductive means in
	either n or p)		direct contact with channel
197	.Bipolar transistor		<pre>(e.g., non-insulated gate)</pre>
198	Wide band gap emitter	218	High resistivity channel
199	.Avalanche diode (e.g., so-called		(e.g., accumulation mode) or
	"Zener" diode having breakdown		surface channel (e.g.,
	voltage greater than 6 volts,		transfer of signal charge
	including heterojunction		occurs at the surface of the
	IMPATT type microwave diodes)		semiconductor) or minority
	IIIIII oppo microwave aroaes)		carriers at input (i.e.,
			surface channel input)
		219	Impurity concentration
			variation
			variacion

257 - 6 CLASS 257 ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID-STATE DIODES)

220	<pre>Vertically within channel (e.g., profiled)</pre>	240	Changing width or direction of channel (e.g., meandering
221	Along the length of the		channel)
	channel (e.g., doping	241	Multiple channels (e.g.,
	variations for transfer		converging or diverging or
	directionality)		parallel channels)
222	Responsive to non-electrical	242	Vertical charge transfer
	external signal (e.g., imager)	243	Channel confinement
223	Having structure to improve	244	Comprising a groove
223	output signal (e.g.,	245	Structure for applying electric
	antiblooming drain)	243	
224	Channel confinement		field into device (e.g.,
225			resistive electrode, acoustic
225	Non-electrical input responsive	0.46	traveling wave in channel)
	(e.g., light responsive	246	Phase structure (e.g., doping
	imager, input programmed by		variations to provide
	size of storage sites for use		asymmetry for 2-phase
	as a read-only memory, etc.)		operation; more than four
226	Sensor element and charge		phases or "electrode per bit")
	transfer device are of	247	Uniphase or virtual phase
	different materials or on		structure
	different substrates (e.g.,	248	2-phase
	"hybrid")	249	Electrode structures or
227	With specified dopant (e.g.,		materials
	photoionizable, "extrinsic"	250	Plural gate levels
	detectors for infrared)	251	Substantially incomplete signal
228	Light responsive, back		charge transfer (e.g., bucket
	illuminated		brigade)
229	Having structure to improve	252	.Responsive to non-optical, non-
	output signal (e.g., exposure		electrical signal
	control structure)	253	Chemical (e.g., ISFET, CHEMFET)
230	With blooming suppression	254	Physical deformation (e.g.,
	structure	234	strain sensor, acoustic wave
231	2-dimensional area		detector)
	architecture	255	,
232	Having alternating strips of	255	.With current flow along
252	sensor structures and register		specified crystal axis (e.g.,
	structures (e.g., interline		axis of maximum carrier
	imager)	056	mobility)
222		256	.Junction field effect transistor
233	Sensors not overlaid by		(unipolar transistor)
224	electrode (e.g., photodiodes)	257	Light responsive or combined
234	Single strip of sensors (e.g.,		with light responsive device
	linear imager)	258	In imaging array
235	Electrical input	259	Elongated active region acts as
236	Signal applied to field effect		transmission line or
	electrode		distributed active element
237	Charge-presetting/linear		(e.g., "transmission line"
	input type (e.g., fill and		field effect transistor)
	spill)	260	Same channel controlled by both
238	Input signal responsive to		junction and insulated gate
	signal charge in charge		electrodes, or by both
	transfer device (e.g.,		Schottky barrier and pn
	regeneration or feedback)		junction gates (e.g., "taper
239	Signal charge detection type		isolated" memory cell)
	(e.g., floating diffusion or		
	floating gate non-destructive		
	output)		

261	Junction gate region free of	284	Schottky gate in groove
	direct electrical connection	285	With profiled channel dopant
	(e.g., floating junction gate		concentration or profiled gate
	memory cell structure)		region dopant concentration
262	Combined with insulated gate		(e.g., maximum dopant
	field effect transistor		concentration below surface)
	(IGFET)	286	With non-uniform channel
262	,	200	
263	Vertical controlled current	005	thickness or width
	path	287	With multiple channels or
264	Enhancement mode or with high		channel segments connected in
	resistivity channel (e.g.,		parallel, or with channel much
	doping of 10 15 cm -3 or less)		wider than length between
265	In integrated circuit		source and drain (e.g., power
266	With multiple parallel current		JFET)
	paths (e.g., grid gate)	288	.Having insulated electrode
267	With Schottky barrier gate		(e.g., MOSFET, MOS diode)
268	Enhancement mode	289	Significant semiconductor
269	With means to adjust barrier		chemical compound in bulk
209	3		crystal (e.g., GaAs)
0.00	height (e.g., doping profile)	290	Light responsive or combined
270	Plural, separately connected,	250	with light responsive device
	gates control same channel	291	Imaging array
	region		
271	Load element or constant	292	Photodiodes accessed by FETs
	current source (e.g., with	293	Photoresistors accessed by
	source to gate connection)		FETs, or photodetectors
272	Junction field effect		separate from FET chip
	transistor in integrated	294	With shield, filter, or lens
	circuit	295	With ferroelectric material
273	With bipolar device		layer
274	Complementary junction field	296	Insulated gate capacitor or
	effect transistors		insulated gate transistor
275	Microwave integrated circuit		combined with capacitor (e.g.,
2.0	(e.g., microstrip type)		dynamic memory cell)
276	With contact or heat sink	297	With means for preventing
270	extending through hole in		charge leakage due to minority
			carrier generation (e.g.,
	semiconductor substrate, or		alpha generated soft error
	with electrode suspended over		protection or "dark current"
	substrate (e.g., air bridge)		leakage protection)
277	With capacitive or inductive	200	Capacitor for signal storage
	elements	298	_
278	With devices vertically spaced		in combination with non-
	in different layers of	000	volatile storage means
	semiconductor material (e.g.,	299	Structure configured for
	"3-dimensional" integrated		voltage converter (e.g.,
	circuit)		charge pump, substrate bias
279	Pn junction gate in compound		generator)
	semiconductor material (e.g.,	300	Capacitor coupled to, or forms
	GaAs)		gate of, insulated gate field
280	With Schottky gate		effect transistor (e.g., non-
281	Schottky gate to silicon		destructive readout dynamic
	semiconductor		memory cell structure)
282	Gate closely aligned to source	301	Capacitor in trench
202	region	302	Vertical transistor
202	_	303	Stacked capacitor
283	With groove or overhang for		•
	alignment		

257 - 8 CLASS 257 ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID-STATE DIODES)

304	Storage node isolated by	324	Multiple insulator layers
	dielectric from semiconductor		(e.g., MNOS structure)
205	substrate	325	Non-homogeneous composition
305	With means to insulate		insulator layer (e.g., graded
	adjacent storage nodes (e.g., channel stops or field oxide)		composition layer or layer with inclusions)
306	Stacked capacitor	326	With additional, non-memory
307	Parallel interleaved	320	control electrode or channel
307	capacitor electrode pairs		portion (e.g., accessing field
	(e.g., interdigitized)		effect transistor structure)
308	With capacitor electrodes	327	Short channel insulated gate
	connection portion located		field effect transistor
	centrally thereof (e.g., fin	328	Vertical channel or double
	electrodes with central post)		diffused insulated gate field
309	With increased effective		effect device provided with
	electrode surface area (e.g.,		means to protect against
	tortuous path, corrugated, or		excess voltage (e.g., gate
	textured electrodes)		protection diode)
310	With high dielectric constant	329	Gate controls vertical charge
	insulator (e.g., Ta 2 0 5)		flow portion of channel (e.g.,
311	Storage Node isolated by	330	VMOS device)
	dielectric from semiconductor substrate	331	Gate electrode in groovePlural gate electrodes or
312	Voltage variable capacitor (i.	331	grid shaped gate electrodes or
312	e., capacitance varies with	332	Gate electrode self-aligned
	applied voltage)	332	with groove
313	Inversion layer capacitor	333	With thick insulator to
314	Variable threshold (e.g.,	333	reduce gate capacitance in
	floating gate memory device)		non-channel areas (e.g., thick
315	With floating gate electrode		oxide over source or drain
316	With additional contacted		region)
	control electrode	334	In integrated circuit
317	With irregularities on		structure
	electrode to facilitate	335	Active channel region has a
	charging or discharging of		graded dopant concentration
	floating electrode		decreasing with distance from
318	Additional control electrode		source region (e.g., double diffused device, DMOS
	is doped region in		transistor)
210	semiconductor substrate	336	With lightly doped portion of
319	Plural additional contacted control electrodes	330	drain region adjacent channel
320	Separate control electrodes		(e.g., LDD structure)
320	for charging and for	337	In integrated circuit
	discharging floating electrode		structure
321	With thin insulator region	338	With complementary field
	for charging or discharging		effect transistor
	floating electrode by quantum	339	With means to increase
	mechanical tunneling		breakdown voltage
322	With charging or discharging	340	\ldots With means (other than self-
	by control voltage applied to		alignment of the gate
	source or drain region (e.g.,		electrode) to decrease gate
	by avalanche breakdown of		capacitance (e.g., shield
202	drain junction)	2/11	electrode)
323	With means to facilitate	341	Plural sections connected in parallel (e.g., power MOSFET)
	light erasure		Pararrer (e.g., power Mosrel)

342	With means to reduce ON resistance	360	Protection device includes insulated gate transistor
343	All contacts on same surface (e.g., lateral structure)		structure (e.g., combined with resistor element)
344	With lightly doped portion of drain region adjacent channel	361	<pre>For operation as bipolar or punchthrough element</pre>
345	<pre>(e.g., LDD structure)With means to prevent sub-</pre>	362	Punchthrough or bipolar element
	<pre>surface currents, or with non- uniform channel doping</pre>	363 364	Including resistor elementWith resistive gate electrode
346	Gate electrode overlaps the source or drain by no more than depth of source or drain	365	With plural, separately connected, gate electrodes in same device
2.45	(e.g., self-aligned gate)	366	Overlapping gate electrodes
347	Single crystal semiconductor layer on insulating substrate (SOI)	367	<pre>Insulated gate controlled breakdown of pn junction (e.g., field plate diode)</pre>
348	Depletion mode field effect transistor	368	Insulated gate field effect transistor in integrated
349	With means (e.g., a buried	260	circuit
	channel stop layer) to prevent leakage current along the	369	Complementary insulated gate field effect transistors
	interface of the semiconductor layer and the insulating	370	Combined with bipolar transistor
2=2	substrate	371	Complementary transistors in
350	Insulated electrode device is combined with diverse type device (e.g., complementary MOSFETs, FET with resistor, etc.)		wells of opposite conductivity types more heavily doped than the substrate region in which they are formed, e.g., twin wells
351	<pre>Complementary field effect transistor structures only (i.e., not including bipolar</pre>	372	With means to prevent latchup or parasitic conduction channels
	transistors, resistors, or other components)	373	With pn junction to collect injected minority carriers to
352	Substrate is single crystal insulator (e.g., sapphire or		prevent parasitic bipolar transistor action
	spinel)	374	Dielectric isolation means
353	Single crystal islands of semiconductor layer containing		<pre>(e.g., dielectric layer in vertical grooves)</pre>
	only one active device	375	With means to reduce
354	Including means to eliminate island edge effects (e.g., insulating filling between		<pre>substrate spreading resistance (e.g., heavily doped substrate)</pre>
	islands, or ions in island edges)	376	With barrier region of
355	With overvoltage protective means		reduced minority carrier lifetime (e.g., heavily doped P+ region to reduce electron
356	For protecting against gate insulator breakdown		minority carrier lifetime, or containing deep level impurity
357	In complementary field effect transistor integrated circuit		or crystal damage), or with region of high threshold
358	Including resistor element		voltage (e.g., heavily doped
359	As thin film structure (e.g., polysilicon resistor)		channel stop region)

257 - 10 CLASS 257 ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID-STATE DIODES)

377	With polysilicon interconnections to source or	394	With means to prevent parasitic conduction channels
	drain regions (e.g.,	395	Thick insulator portion
	<pre>polysilicon laminated with silicide)</pre>	396	Recessed into semiconductor surface
378	Combined with bipolar	397	In vertical-walled groove
	transistor	398	_
379	Combined with passive	390	Combined with heavily doped
375	components (e.g., resistors)	200	channel stop portion
380		399	Combined with heavily doped
	Polysilicon resistor		channel stop portion
381	With multiple levels of	400	With heavily doped channel
	polycrystalline silicon		stop portion
382	With contact to source or	401	With specified physical layout
	drain region of refractory		(e.g., ring gate, source/drain
	material (e.g., polysilicon,		regions shared between plural
	tungsten, or silicide)		FETs, plural sections
383	Contact of refractory or		connected in parallel to form
	platinum group metal (e.g.,		power MOSFET)
	molybdenum, tungsten, or	402	With permanent threshold
	titanium)		adjustment (e.g., depletion
384	Including silicide		mode)
385	Multiple polysilicon layers	403	With channel conductivity
386	With means to reduce parasitic		dopant same type as that of
	capacitance		source and drain
387	Gate electrode overlaps at	404	Non-uniform channel doping
	least one of source or drain	405	With gate insulator containing
	by no more than depth of		specified permanent charge
	source or drain (e.g., self-	406	Plural gate insulator layers
	aligned gate)	407	With gate electrode of
388	Gate electrode consists of	107	controlled workfunction
	refractory or platinum group		material (e.g., low
	metal or silicide		workfunction gate material)
389	With thick insulator over	408	Including lightly doped drain
302	source or drain region	400	portion adjacent channel
390	Matrix or array of field		(e.g., lightly doped drain,
370	effect transistors (e.g.,		LDD device)
	array of FETs only some of	409	With means to increase
	which are completed, or	409	
	structure for mask programmed		breakdown voltage (e.g., field
	read-only memory (ROM))		shield electrode, guard ring,
391	Selected groups of complete	410	etc.)
371	field effect devices having	410	Gate insulator includes
	different threshold voltages		material (including air or
	(e.g., different channel	4.7.7	vacuum) other than SiO 2
	dopant concentrations)	411	Composite or layered gate
392	Insulated gate field effect		insulator (e.g., mixture such
392	transistors of different		as silicon oxynitride)
	threshold voltages in same	412	Gate electrode of refractory
	integrated circuit (e.g.,		material (e.g., polysilicon or
	_		a silicide of a refractory or
	enhancement and depletion mode)	4.4	platinum group metal)
303	•	413	Polysilicon laminated with
393	Insulated gate field effect		silicide
	transistor adapted to function		
	as load element for switching		
	insulated gate field effect		
	transistor		

414	RESPONSIVE TO NON-ELECTRICAL SIGNAL (E.G., CHEMICAL, STRESS, LIGHT, OR MAGNETIC FIELD SENSORS)	436	With means for increasing light absorption (e.g., redirection of unabsorbed light)
415	.Physical deformation	437	Antireflection coating
416	Acoustic wave	438	Avalanche junction
417	Strain sensors	439	Containing dopant adapted for
418	With means to concentrate		photoionization
	stress	440	With different sensor portions
419	With thinned central active portion of semiconductor surrounded by thick		responsive to different wavelengths (e.g., color imager)
	insensitive portion (e.g. diaphragm type strain gauge)	441	Narrow band gap semiconductor (< <lev) (e.g.,="" pbsnte)<="" td=""></lev)>
420	Means to reduce sensitivity to physical deformation	442	<pre>II-VI compound semiconductor (e.g., HgCdTe)</pre>
421	.Magnetic field	443	Matrix or array (e.g., single
422	With magnetic field directing		line arrays)
400	<pre>means (e.g., shield, pole piece, etc.)</pre>	444	Light sensor elements overlie active switching elements in
423	<pre>Bipolar transistor magnetic field sensor (e.g., lateral bipolar transistor)</pre>		<pre>integrated circuit (e.g., where the sensor elements are deposited on an integrated</pre>
424	Sensor with region of high		circuit)
	carrier recombination (e.g.,	445	With antiblooming means
	magnetodiode with carriers deflected to recombination	446	With specific isolation means in integrated circuit
405	region by magnetic field)	447	With backside illumination
425	<pre>Magnetic field detector using compound semiconductor material (e.g., GaAs, InSb,</pre>		<pre>(e.g., having a thinned central area or a non- absorbing substrate)</pre>
	etc.)	448	With particular electrode
426	Differential output (e.g., with	110	configuration
	offset adjustment means or	449	Schottky barrier (e.g., a
	with means to reduce temperature sensitivity)	119	transparent Schottky metallic layer or a Schottky barrier
427	Magnetic field sensor in integrated circuit (e.g., in		containing at least one of indium or tin (e.g., SnO 2 ,
	bipolar transistor integrated	450	indium tin oxide))
428	circuit) .Electromagnetic or particle	450	<pre>With doping profile to adjust barrier height</pre>
400	radiation	451	Responsive to light having
429	Charged or elementary particles		lower energy (i.e., longer
430	With active region having effective impurity		wavelength) than forbidden band gap energy of
421	concentration less than 10 12 atoms/cm 3		<pre>semiconductor (e.g., by excitation of carriers from metal into semiconductor)</pre>
431	Light	452	•
432	With optical element	452	With edge protection, e.g.,
433	With housing or encapsulation		doped guard ring or mesa
434	With window means	452	structure
435	With optical shield or mask means	453	With specified Schottky metallic layer
		454	Schottky metallic layer is a silicide

257 - 12 CLASS 257 ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID-STATE DIODES)

455	Silicide of Platinum group metal	480	.In voltage variable capacitance diode
456	Silicide of refractory	481	.Avalanche diode (e.g., so-called "Zener" diode having breakdown
4 - 7			
457	With particular contact	482	voltage greater than 6 volts)Microwave transit time device
450	geometry (e.g., ring or grid)	402	
458	PIN detector, including	402	(e.g., IMPATT diode)
	combinations with non-light	483	.With means to prevent edge breakdown
450	responsive active devices	404	
459	With particular contact	484	Guard ring
	geometry (e.g., ring or grid,	485	.Specified materials
460	or bonding pad arrangement)With backside illumination	486	Layered (e.g., a diffusion
400	(e.g., with a thinned central		barrier material layer or a
	area or non-absorbing		silicide layer or a precious metal layer)
	substrate)	487	WITH MEANS TO INCREASE BREAKDOWN
461	Light responsive pn junction	407	VOLTAGE THRESHOLD
462	Phototransistor	488	.Field relief electrode
463	With particular doping	489	Resistive
103	concentration	490	ResistiveCombined with floating pn
464	With particular layer	470	junction guard region
101	thickness (e.g., layer less	491	.In integrated circuit
	than light absorption depth)	492	With electric field controlling
465	Geometric configuration of	1/2	semiconductor layer having a
	junction (e.g., fingers)		low enough doping level in
466	External physical		relationship to its thickness
	configuration of semiconductor		to be fully depleted prior to
	(e.g., mesas, grooves)		avalanche breakdown (e.g.,
467	.Temperature		RESURF devices)
468	Semiconductor device operated	493	.With electric field controlling
	at cryogenic temperature		semiconductor layer having a
469	With means to reduce		low enough doping level in
	temperature sensitivity (e.g.,		relationship to its thickness
	reduction of temperature		to be fully depleted prior to
	sensitivity of junction		avalanche breakdown (e.g.,
	breakdown voltage by using a	40.4	RESURF devices)
	compensating element)	494	.Reverse-biased pn junction guard
470	Pn junction adapted as	405	region
	temperature sensor	495	.Floating pn junction guard
471	SCHOTTKY BARRIER	100	region
472	.To compound semiconductor	496	.With physical configuration of semiconductor surface to
473	With specified Schottky metal		reduce electric field (e.g.,
474	.As active junction in bipolar		reverse bevels, double bevels,
	transistor (e.g., Schottky		stepped mesas, etc.)
475	collector)	497	PUNCHTHROUGH STRUCTURE DEVICE
475	.With doping profile to adjust	10 /	(E.G., PUNCHTHROUGH
176	barrier height		TRANSISTOR, CAMEL BARRIER
476 477	.In integrated structure		DIODE)
	With bipolar transistor	498	.Punchthrough region fully
478	Plural Schottky barriers with different barrier heights		depleted at zero external
479	Connected across base-		applied bias voltage (e.g.,
ユノン	collector junction of		camel barrier or planar doped
	transistor (e.g., Baker clamp)		barrier devices, or so-called
	orange (c.g., paner cramp)		"Bipolar SIT" devices)

499	INTEGRATED CIRCUIT STRUCTURE WITH ELECTRICALLY ISOLATED COMPONENTS	514	<pre>With active junction abutting groove (e.g., "walled emitter")</pre>
500	.Including high voltage or high power devices isolated from low voltage or low power	515	<pre>With active junction abutting groove (e.g., "walled emitter")</pre>
	devices in the same integrated circuit	516	<pre>With passive component (e.g., resistor, capacitor, etc.)</pre>
501	Including dielectric isolation means	517	With bipolar transistor structure
502	High power or high voltage device extends completely through semiconductor	518	With polycrystalline connecting region (e.g., polysilicon base contact)
503	<pre>substrate (e.g., backside collector contact) .With contact or metallization</pre>	519	Including heavily doped channel stop region adjacent
503	configuration to reduce parasitic coupling (e.g., separate ground pads for	520	grooveConductive filling in dielectric-lined groove (e.g., polysilicon backfill)
504	<pre>different parts of integrated circuit) .Including means for establishing</pre>	521	Sides of grooves along major crystal planes (e.g., (111),
	a depletion region throughout a semiconductor layer for isolating devices in different	522	<pre>(100) planes, etc.)Air isolation (e.g., beam lead supported semiconductor islands)</pre>
	<pre>portions of the layer (e.g., "JFET" isolation)</pre>	523	Isolation by region of intrinsic (undoped)
505	.With polycrystalline semiconductor isolation region in direct contact with single		semiconductor material (e.g., including region physically damaged by proton bombardment)
506	<pre>crystal active semiconductor material .Including dielectric isolation</pre>	524	Full dielectric isolation with polycrystalline semiconductor
	means	525	<pre>substrateWith complementary (npn and</pre>
507	<pre>With single crystal insulating substrate (e.g., sapphire)</pre>	323	pnp) bipolar transistor
508	With metallic conductor within isolating dielectric or	526	With bipolar transistor structure
	between semiconductor and isolating dielectric (e.g., metal shield layer or internal connection layer)	527	<pre>Sides of isolated semiconductor islands along major crystal planes (e.g., (111), (100) planes, etc.)</pre>
509	Combined with pn junction	528	.Passive components in ICs
	isolation (e.g., isoplanar, LOCOS)	529	Including programmable passive component (e.g., fuse)
510	Dielectric in groove	530	Anti-fuse
511	With complementary (npn and	531	Including inductive element
	pnp) bipolar transistor	532	Including capacitor component
512	structures	533	Combined with resistor to form
) I Z	Complementary devices share common active region (e.g.,		RC filter structure
	integrated injection logic, I 2 L)	534	With means to increase surface area (e.g., grooves, ridges,
513	Vertical walled groove	535	etc.)Both terminals of capacitor isolated from substrate

257 - 14 CLASS 257 ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID-STATE DIODES)

536 537	<pre>Including resistive elementUsing specific resistive material</pre>	551	Including voltage reference element (e.g., avalanche diode, so-called "Zener diode"
538	Polycrystalline silicon (doped or undoped)		with breakdown voltage greater than 6 volts or with positive
539	Combined with bipolar transistor	552	temperature coefficient of breakdown voltage)
540	With compensation for non- linearity (e.g., dynamic	552	With bipolar transistor structureTransistors of same
541 542	<pre>isolation pocket bias)Pinch resistorResistor has same doping as</pre>	333	conductivity type (e.g., npn) having different current gain
	emitter or collector of bipolar transistor	554	or different operating voltage characteristics
543	<pre>Lightly doped junction isolated resistor (e.g., ion implanted resistor)</pre>	554	With connecting region made of polycrystalline semiconductor material (e.g., polysilicon base contact)
544 545	<pre>.With pn junction isolationWith means to control isolation junction capacitance (e.g., lightly doped layer at</pre>	555	Complementary bipolar transistor structures (e.g., integrated injection logic, I
	isolation junction to increase depletion layer width)	556	<pre>2 L)Including lateral bipolar transistor structure</pre>
546	With structural means to protect against excess or	557	.Lateral bipolar transistor structure
547	reversed polarity voltageWith structural means to control parasitic transistor action or leakage current	558	With base region doping concentration step or gradient or with means to increase
548	At least three regions of alternating conductivity types with dopant concentration	559	current gain With active region formed along groove or exposed edge in semiconductor
	<pre>gradients decreasing from surface of semiconductor (e.g., "triple-diffused"</pre>	560	With multiple collectors or emitters
549	integrated circuit)With substrate and lightly	561	With different emitter to collector spacings or facing
	doped surface layer of same conductivity type, separated	562	<pre>areasWith auxiliary collector/re-</pre>
	<pre>by subsurface heavily doped region of opposite conductivity type (e.g., "collector diffused isolation"</pre>		<pre>emitter between emitter and output collector (e.g., "Current Hogging Logic" device)</pre>
550	<pre>integrated circuit)With lightly doped surface layer of one conductivity type</pre>	563	.With multiple separately connected emitter, collector, or base regions in same
	on substrate of opposite conductivity type, having	564	transistor structureMultiple base or collector
	plural heavily doped portions of the one conductivity type between the layer and substrate, different ones of the heavily doped portions having differing depths or	565 566	regions BIPOLAR TRANSISTOR STRUCTURE .Plural non-isolated transistor structures in same structure
	physical extent		

567	Darlington configuration (i.e., emitter to collector current of input transistor supplied to base region of output transistor)	583	With means to reduce transistor action in selected portions of transistor (e.g., heavy base region doping under central web of emitter to prevent
568	More than two Darlington- connected transistors	584	secondary breakdown)With housing or contact (i.e.,
569 570	Complementary Darlington- connected transistors With active components in	585	electrode) means .With means to increase inverse gain
370	addition to Darlington transistors (e.g., antisaturation diode, bleeder diode connected antiparallel to input transistor base-	586 587 588	.With non-planar semiconductor surface (e.g., groove, mesa, bevel, etc.).With specified electrode means.Including polycrystalline
	emitter junction, etc.)		semiconductor as connection
571	Non-planar structure (e.g.,	589	.Avalanche transistor
	mesa emitter, or having a	590	.With means to reduce minority
572	<pre>groove to define resistor)With resistance means connected between transistor</pre>		carrier lifetime (e.g., region of deep level dopant or region of crystal damage)
	base regions	591	.With emitter region having
573	With housing or contact structure or configuration		specified doping concentration profile (e.g., high-low
574	Complementary transistors share		concentration step)
	<pre>common active region (e.g., integrated injection logic, I 2 L)</pre>	592	.With base region having specified doping concentration profile or specified
575	Including lateral bipolar transistor structure		configuration (e.g., inactive base more heavily doped than
576	<pre>With contacts of refractory material (e.g., polysilicon, silicide of refractory or platinum group metal)</pre>		active base or base region has constant doping concentration portion (e.g., epitaxial base))
577	.Including additional component in same, non-isolated	593	.With means to increase current gain or operating frequency
	structure (e.g., transistor with diode, transistor with	594	WITH GROOVE TO DEFINE PLURAL DIODES
	resistor, etc.)	595	VOLTAGE VARIABLE CAPACITANCE
578	.With enlarged emitter area		DEVICE
	(e.g., power device)	596	.With specified dopant profile
579	With separate emitter areas connected in parallel	597	Retrograde dopant profile (e.g., dopant concentration
580	With current ballasting means (e.g., emitter ballasting		decreases with distance from rectifying junction)
	resistors or base current ballasting means)	598	.With plural junctions whose depletion regions merge to
581	Thin film ballasting means		vary voltage dependence
	(e.g., polysilicon resistor)	599	.With means to increase active
582	With current ballasting means		junction area (e.g., grooved
	(e.g., emitter ballasting		or convoluted surface)
	resistors or base current ballasting resistors)	600	<pre>.With physical configuration to vary voltage dependence (e.g., mesa)</pre>

257 - 16 CLASS 257 ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID-STATE DIODES)

601	.Plural diodes in same non- isolated structure, or device having three or more terminals	621	.With electrical contact in hole in semiconductor (e.g., lead extends through semiconductor
602	.With specified housing or	622	body)
600	contact		Groove
603	AVALANCHE DIODE (E.G., SO-CALLED "ZENER" DIODE HAVING BREAKDOWN VOLTAGE GREATER THAN 6 VOLTS)	623	.Mesa structure (e.g., including undercut or stepped mesa configuration or having
604	<pre>.Microwave transit time device (e.g., IMPATT diode)</pre>	624	<pre>constant slope taper)With low resistance ohmic</pre>
605	.With means to limit area of breakdown (e.g., guard ring having higher breakdown voltage)		connection means along exposed mesa edge (e.g., contact or heavily doped region along exposed mesa to region along
606	Subsurface breakdown		effect" losses in microwave
607	WITH SPECIFIED DOPANT (E.G.,		diode)
	PLURAL DOPANTS OF SAME CONDUCTIVITY IN SAME REGION)	625	Semiconductor body including mesa is intimately bonded to
608	.Switching device based on filling and emptying of deep energy levels		thick electrical and/or thermal conductor member of larger lateral extent than
609	<pre>.For compound semiconductor (e.g., deep level dopant)</pre>		<pre>semiconductor body (e.g., "plated heat sink" microwave</pre>
610	.Deep level dopant		diode)
611	With specified distribution	626	Combined with passivating
	(e.g., laterally localized,		coating
	with specified concentration distribution or gradient)	627	.With specified crystal plane or axis
612	Deep level dopant other than gold or platinum	628	Major crystal plane or axis other than (100), (110), or
613	INCLUDING SEMICONDUCTOR MATERIAL OTHER THAN SILICON OR GALLIUM		(111) (e.g., (731) axis, crystal plane several degrees
	ARSENIDE (GAAS) (E.G., PB X SN 1-X TE)	629	from (100) toward (011), etc.) WITH MEANS TO CONTROL SURFACE
614	.Group II-VI compound (e.g.,		EFFECTS
	CdTe, Hg x Cd 1-x Te)	630	.With inversion-preventing shield electrode
615	.Group III-V compound (e.g., InP)	631	.In compound semiconductor
616	.Containing germanium, Ge	031	material (e.g., GaAs)
617	INCLUDING REGION CONTAINING	632	
	CRYSTAL DAMAGE		.Insulating coating
618	PHYSICAL CONFIGURATION OF	633	With thermal expansion
	SEMICONDUCTOR (E.G., MESA,		compensation (e.g., thermal
	BEVEL, GROOVE, ETC.)		expansion of glass passivant
619	.With thin active central		matched to that of
	semiconductor portion		semiconductor)
	surrounded by thicker inactive	634	Insulating coating of glass
	shoulder (e.g., for mechanical		composition containing
	support)		component to adjust melting or
620			softening temperature (e.g.,
UZU	.With peripheral feature due to		low melting point glass)
	separation of smaller	635	Multiple layers
	semiconductor chip from larger	636	At least one layer of semi-
	wafer (e.g., scribe region, or		insulating material
	means to prevent edge effects	627	_
	such as leakage current at	637	Three or more insulating
	peripheral chip separation		layers
	area)		
	•		

638	With discontinuous or varying thickness layer (e.g., layer covers only selected portions	660	.With means to shield device contained in housing or package from charged particles
	of semiconductor)		(e.g., alpha particles) or
639	At least one layer of silicon		highly ionizing radiation
037	oxynitride		(i.e., hard X-rays or shorter
640	At least one layer of silicon		wavelength)
010	nitride	661	SUPERCONDUCTIVE CONTACT OR LEAD
641	Combined with glass layer	662	.Transmission line or shielded
642		663	On integrated circuit
042	At least one layer of organic material	664	TRANSMISSION LINE LEAD (E.G.,
612		004	STRIPLINE, COAX, ETC.)
643 644	Polyimide or polyamide	665	CONTACTS OR LEADS INCLUDING
	At least one layer of glass	003	FUSIBLE LINK MEANS OR NOISE
645	Insulating layer containing		SUPPRESSION MEANS
	specified electrical charge	666	LEAD FRAME
	(e.g., net negative electrical	667	
C 1 C	charge)		.With dam or vent for encapsulant
646	<pre>Coating of semi-insulating material (e.g., amorphous</pre>	668	.On insulating carrier other than a printed circuit board
	silicon or silicon-rich	669	.With stress relief
	silicon oxide)	670	.With separate tie bar element or
647	Insulating layer recessed into		plural tie bars
	semiconductor surface (e.g.,	671	Of insulating material
	LOCOS oxide)	672	.Small lead frame (e.g., "spider"
648	Combined with channel stop		frame) for connecting a large
	region in semiconductor		lead frame to a semiconductor
649	Insulating layer of silicon		chip
	nitride or silicon oxynitride	673	.With bumps on ends of lead
650	Insulating layer of glass		fingers to connect to
651	Details of insulating layer		semiconductor
	electrical charge (e.g.,	674	.With means for controlling lead
	negative insulator layer		tension
	charge)	675	.With heat sink means
652	.Channel stop layer	676	.With structure for mounting
653	WITH SPECIFIED SHAPE OF PN		semiconductor chip to lead
	JUNCTION		frame (e.g., configuration of
654	.Interdigitated pn junction or		die bonding flag, absence of a
001	more heavily doped side of		die bonding flag, recess for
	junction is concave		LED)
655	WITH SPECIFIED IMPURITY	677	.Of specified material other than
033	CONCENTRATION GRADIENT		copper (e.g., Kovar (T.M.))
656	.With high resistivity (e.g.,	678	HOUSING OR PACKAGE
050	"intrinsic") layer between P	679	.Smart (e.g., credit) card
	and N layers (e.g., PIN diode)	015	package
657	.Stepped profile	680	.With window means
658		681	For erasing EPROM
	PLATE TYPE RECTIFIER ARRAY		_
659	WITH SHIELDING (E.G., ELECTRICAL	682	.With desiccant, getter, or gas
	OR MAGNETIC SHIELDING, OR FROM	602	filling
	ELECTROMAGNETIC RADIATION OR	683	.With means to prevent explosion
	CHARGED PARTICLES)		of package
		684	.With semiconductor element
			forming part (e.g., base, of
			housing)
		685	.Multiple housings
		686	Stacked arrangement

257 - 18 CLASS 257 ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID-STATE DIODES)

687	.Housing or package filled with solid or liquid electrically	717	Isolation of cooling means (e.g., heat sink) by an
	insulating material		electrically insulating
688	.With large area flexible	E1.0	element (e.g., spacer)
	electrodes in press contact	718	Heat dissipating element held
	with opposite sides of active		in place by clamping or spring
	semiconductor chip and	710	means
	surrounded by an insulating	719	Pressed against semiconductor
600	element, e.g., ring	500	element
689	Rigid electrode portion	720	Heat dissipating element has
690	.With contact or lead		high thermal conductivity
691	<pre>Having power distribution means (e.g., bus structure)</pre>		<pre>insert (e.g., copper slug in aluminum heat sink)</pre>
692	With particular lead geometry	721	With gas coolant
693	External connection to housing	722	With fins
694	Axial leads	723	.For plural devices
695	Fanned/radial leads	724	With discrete components
696	Bent (e.g., J-shaped) lead	725	With electrical isolation means
697	Pin grid type	726	Devices held in place by
698	With specific electrical		clamping
	feedthrough structure	727	.Device held in place by clamping
699	Housing entirely of metal	728	.For high frequency (e.g.,
	except for feedthrough		microwave) device
	structure	729	.Portion of housing of specific
700	Multiple contact layers		materials
	separated from each other by	730	.Outside periphery of package
	insulator means and forming		having specified shape or
	part of a package or housing		configuration
	(e.g., plural ceramic layer	731	.With housing mount
	package)	732	Flanged mount
701	.Insulating material	733	Stud mount
702	Of insulating material other	734	COMBINED WITH ELECTRICAL CONTACT
	than ceramic		OR LEAD
703	Composite ceramic, or single	735	.Beam leads (i.e., leads that
	ceramic with metal		extend beyond the ends or
704	Cap or lid		sides of a chip component)
705	Of high thermal conductivity	736	Layered
	ceramic (e.g., BeO)	737	.Bump leads
706	With heat sink	738	Ball shaped
707	Directly attached to	739	.With textured surface
	semiconductor device	740	.With means to prevent contact
708	.Entirely of metal except for		from penetrating shallow PN
	feedthrough		junction (e.g., prevention of
709	With specified insulator to		aluminum "spiking")
	isolate device from housing	741	.Of specified material other than
710	With specified means (e.g.,		unalloyed aluminum
	lip) to seal base to cap	742	With a semiconductor
711	With raised portion of base for		conductivity substitution type
	mounting semiconductor chip		dopant (e.g., germanium in the
712	.With provision for cooling the		case of a gallium arsenide
	housing or its contents		semiconductor) in a contact
713	For integrated circuit	712	metal)
714	Liquid coolant	743	For compound semiconductor
715	Boiling (evaporative) liquid		material
716	Cryogenic liquid coolant		

744	For compound semiconductor material	766	At least one layer containing chromium or nickel
745	Contact for III-V material	767	Resistive to electromigration
746	Composite material (e.g.,		or diffusion of the contact or
	fibers or strands embedded in		lead material
	solid matrix)	768	Refractory or platinum group
747	With thermal expansion matching		metal or alloy or silicide
	of contact or lead material to		thereof
	semiconductor active device	769	Platinum group metal or
748	Plural layers of specified		silicide thereof
	contact or lead material	770	Molybdenum, tungsten, or
749	At least portion of which is		titanium or their silicides
	transparent to ultraviolet,	771	Alloy containing aluminum
	visible or infrared light	772	Solder composition
750	Layered	773	.Of specified configuration
751	At least one layer forms a	774	Via (interconnection hole)
	diffusion barrier		shape
752	Planarized to top of	775	Varying width or thickness of
	insulating layer		conductor
753	With adhesion promoting means	776	Cross-over arrangement,
	(e.g., layer of material) to		component or structure
	promote adhesion of contact to	777	.Chip mounted on chip
	an insulating layer	778	.Flip chip
754	At least one layer of silicide	779	.Solder wettable contact, lead,
	or polycrystalline silicon		or bond
755	Polysilicon laminated with	780	.Ball or nail head type contact,
	silicide		lead, or bond
756	Multiple polysilicon layers	781	Layered contact, lead or bond
757	Silicide of refractory or	782	.Die bond
	platinum group metal	783	With adhesive means
758	Multiple metal levels on	784	.Wire contact, lead, or bond
	semiconductor, separated by	785	.By pressure alone
	insulating layer (e.g.,	786	.Configuration or pattern of
	multiple level metallization		bonds
==0	for integrated circuit)	787	ENCAPSULATED
759	Including organic insulating	788	.With specified encapsulant
E.C.O.	material between metal levels	789	With specified filler material
760	Separating insulating layer	790	Plural encapsulating layers
	is laminate or composite of	791	Including polysiloxane (e.g.,
	plural insulating materials		silicone resin)
	(e.g., silicon oxide on	792	Including polyimide
	<pre>silicon nitride, silicon oxynitride)</pre>	793	Including epoxide
761	At least one layer containing	794	Including glass
701	vanadium, hafnium, niobium,	795	.With specified filler material
	zirconium, or tantalum	796	.With heat sink embedded in
762	At least one layer containing		encapsulant
102	silver or copper	797	ALIGNMENT MARKS
763	At least one layer of	798	MISCELLANEOUS
, 0 5	molybdenum, titanium, or		
	tungsten		
764	Alloy containing molybdenum,		
, 0 1	titanium, or tungsten	E-SUBC	LASSES
765	At least one layer of an alloy		
	containing aluminum		

The following subclasses beginning with the letter E are E-subclasses. Each E-subclass corresponds to a classification in the European Classification system (ECLA). The ECLA classification is parenthesized at the end of the title. E-subclasses contain both U.S. and foreign documents. New U.S. documents are classified here by the USPTO, and European foreign by the EPO. E-subclasses may contain subject matter outside the scope of this class. Consult their definitions, or the documents themselves to clarify or interpret titles.

- E47.001 BULK NEGATIVE RESISTANCE EFFECT
 DEVICES, E.G., GUNN-EFFECT
 DEVICES, PROCESSES, OR
 APPARATUS PECULIAR TO
 MANUFACTURE OR TREATMENT OF
 SUCH DEVICES, OR OF PARTS
 THEREOF (EPO)
- E47.002 .Gunn-effect devices or transferred electron devices (EPO)
- E47.003 ..Controlled by electromagnetic radiation (EPO)
- E47.004 ..Gunn diodes (EPO)
- E47.005 .Processes or apparatus peculiar to manufacture or treatment of these devices or of parts thereof (EPO)
- E39.001 DEVICES USING SUPERCONDUCTIVITY,

 PROCESSES, OR APPARATUS

 PECULIAR TO MANUFACTURE OR

 TREATMENT OF SUCH DEVICES, OR

 OF PARTS THEREOF (EPO)
- E39.002 .Containers or mountings (EPO)
- E39.003 .. For Josephson devices (EPO)
- E39.004 .Characterized by current path (EPO)
- E39.005 .Characterized by shape of element (EPO)
- E39.006 .Characterized by material (EPO)
- E39.007 .. Organic materials (EPO)
- E39.008 ...Fullerene superconductors, e.g., soccerball-shaped allotrope of carbon, e.g., C60, C94 (EPO)
- E39.009 ..Ceramic materials (EPO)
- E39.01 ...Comprising copper oxide (EPO)
- E39.011Multilayered structures, e.g., super lattices (EPO)
- E39.012 .Devices comprising junction of dissimilar materials, e.g.,
 Josephson-effect devices (EPO)

- E39.013 ..Single electron tunnelling devices (EPO)
- E39.014 .. Josephson-effect devices (EPO)
- E39.015 ...Comprising high Tc ceramic materials (EPO)
- E39.016 ..Three or more electrode devices, e.g., transistor-like structures (EPO)
- E39.017 .Permanent superconductor devices (EPO)
- E39.018 .. Comprising high Tc ceramic materials (EPO)
- E39.019 ..Three or more electrode devices (EPO)
- E39.02 ...Field-effect devices (EPO)
- E51.001 ORGANIC SOLID STATE DEVICES,

 PROCESSES OR APPARATUS

 PECULIAR TO MANUFACTURE OR

 TREATMENT OF SUCH DEVICES OR

 OF PARTS THEREOF
- E51.002 .Structural detail of device (EPO)
- E51.003 ..Organic solid-state device adapted for rectifying, amplifying, oscillating, or switching, or capacitors or resistors with potential or surface barrier (EPO)
- E51.004 ...Controllable by only signal applied to control electrode (e.g., base of bipolar transistor, gate of field-effect transistor) (EPO)
- E51.005Field-effect device (e.g., TFT, FET) (EPO)
- E51.006Insulated gate field-effect transistor (EPO)
- E51.007Comprising organic gate dielectric (EPO)
- E51.008 ...Controllable only by variation of electric current supplied or only electric potential applied to electrode carrying current to be rectified, amplified, oscillated, or switched (e.g., two terminal device) (EPO)
- E51.009Comprising Schottky junction (EPO)
- E51.01Comprising organic/organic junction (e.g., heterojunction) (EPO)
- E51.011Comprising organic/inorganic heterojunction (EPO)
- E51.012 ..Radiation-sensitive organic solid-state device (EPO)

E51.013	Metal-organic semiconductor-
	metal device (EPO)
E51.014	Comprising bulk heterojunction
	(EDO)

- E51.015 ...Comprising organic/inorganic heterojunction (EPO)
- E51.016Majority carrier device using sensitization of wide band gap semiconductor (e.g., TiO 2) (EPO)
- E51.017 ...Comprising organic semiconductor-organic semiconductor heterojunction (EPO)
- E51.018 ..Light-emitting organic solidstate device with potential or surface barrier (EPO)
- E51.019 ...Electrode (EPO)
- E51.02Encapsulation (EPO)
- E51.021Arrangements for extracting light from device (e.g., Bragg reflector pair) (EPO)
- E51.022 ...Multicolor organic lightemitting device (OLED) (EPO)
- E51.023 ..Molecular electronic device (EPO)
- E51.024 .Selection of material for organic solid-state device (EPO)
- E51.025 ..For organic solid-state device adapted for rectifying, amplifying, oscillating, or switching, or capacitors or resistors with potential or surface barrier (EPO)
- E51.026 ..For radiation-sensitive or light-emitting organic solid-state device with potential or surface barrier (EPO)
- E51.027 ..Organic polymer or oligomer (EPO)
- E51.028 ...Comprising aromatic, heteroaromatic, or arrylic chains (e.g., polyaniline, polyphenylene, polyphenylene vinylene) (EPO)
- E51.029Heteroaromatic compound comprising sulfur or selene (e.g., polythiophene) (EPO)
- E51.03Polyethylene dioxythiophene and derivative (EPO)
- E51.031Polyphenylenevinylene and derivatives (EPO)
- E51.032Polyflurorene and derivative (EPO)

- E51.033 ...Comprising aliphatic or olefinic chains (e.g., polyN-vinylcarbazol, PVC, PTFE) (EPO)
- E51.034Polyacetylene or derivatives (EPO)
- E51.035PolyN-vinylcarbazol and derivative (EPO)
- E51.036 ...Copolymers (EPO)
- E51.037 ...Ladder-type polymer (EPO)
- E51.038 ..Carbon-containing materials (EPO)
- E51.039 ...Fullerenes (EPO)
- E51.04 ... Carbon nanotubes (EPO)
- E51.041 ..Coordination compound (e.g., porphyrin, phthalocyanine, metal(II) polypyridine complexes) (EPO)
- E51.042 ...Phthalocyanine (EPO)
- E51.043 ...Metal complexes comprising
 Group IIIB metal (Al, Ga, In,
 or Ti) (e.g., Tris (8hydroxyquinoline) aluminium
 (Alq3)) (EPO)
- E51.044 ...Transition metal complexes (e.g., Ru(II) polypyridine complexes) (EPO)
- E51.045 ..Biomolecule or macromolecule (e.g., proteins, ATP, chlorophyl, beta-carotene, lipids, enzymes) (EPO)
- E51.046 ..Silicon-containing organic semiconductor (EPO)
- E51.047 ..Macromolecular system with low molecular weight (e.g., cyanine dyes, coumarine dyes, tetrathiafulvalene) (EPO)
- E51.048 ...Charge transfer complexes (EPO)
- E51.049 ...Polycondensed aromatic or heteroaromatic compound (e.g., pyrene, perylene, pentacene) (EPO)
- E51.05Aromatic compound containing heteroatom (e.g., perylenetetracarboxylic dianhydride, perylene tetracarboxylic diimide) (EPO)
- E51.051 ...Amine compound having at least two aryl on amine-nitrogen atom (e.g., triphenylamine) (EPO)
- E51.052 ..Langmuir Blodgett film (EPO)

E43.001 SEMICONDUCTOR OR SOLID-STATE DEVICES USING GALVANO-MAGNETIC	E33.017Characterized by doping material (EPO)
OR SIMILAR MAGNETIC EFFECTS, PROCESSES OR APPARATUS PECULIAR TO MANUFACTURE OR	E33.018Including porous Si (EPO) E33.019Comprising only Group II-VI compound (EPO)
TREATMENT OF SUCH DEVICES, OR OF PARTS THEREOF (EPO)	E33.02Ternary or quaternary compound (e.g., CdHgTe) (EPO)
E43.002 .Hall-effect devices (EPO)	E33.021With heterojunction (EPO)
E43.003Semiconductor Hall-effect	E33.022Characterized by doping
devices (EPO)	material (EPO)
E43.004 .Magnetic-field-controlled resistors (EPO)	E33.023Comprising only Group III-V compound (EPO)
E43.005 .Selection of materials (EPO) E43.006 .Processes or apparatus peculiar	E33.024Binary compound (e.g., GaAs) (EPO)
to manufacture or treatment of these devices or of parts	E33.025Including nitride (e.g., GaN) (EPO)
thereof (EPO) E43.007For Hall-effect devices (EPO)	E33.026Ternary or quaternary
E33.001 LIGHT EMITTING SEMICONDUCTOR	compound (e.g., AlGaAs) (EPO) E33.027With heterojunction (EPO)
DEVICES HAVING A POTENTIAL OR	E33.028Including nitride (e.g.,
A SURFACE BARRIER, PROCESSES	Algan) (EPO)
OR APPARATUS PECULIAR TO THE MANUFACTURE OR TREATMENT OF	E33.029Characterized by doping material (EPO)
SUCH DEVICES, OR OF PARTS THEREOF	E33.03Nitride compound (EPO)
E33.002 .Device characterized by	E33.031Including ternary or
semiconductor body (EPO)	quaternary compound (e.g.,
E33.003Particular crystalline	AlGaAs) (EPO)
orientation or structure (EPO)	E33.032With heterojunction (e.g.,
E33.004Comprising amorphous	AlGaAs/GaAs) (EPO) E33.033Comprising nitride compound
semiconductor (EPO)	(e.g., Algan) (EPO)
E33.005Shape or structure (e.g., shape of epitaxial layer) (EPO)	E33.034With heterojunction (e.g., AlGaN/GaN) (EPO)
E33.006Shape of semiconductor body (EPO)	E33.035Comprising only Group IV compound (e.g., SiC) (EPO)
E33.007Shape of potential barrier (EPO)	E33.036Characterized by doping material (EPO)
E33.008Multiple quantum well	E33.037Comprising compound other than
structure (EPO) E33.009Including, apart from doping	Group II-VI, III-V, and IV compound (EPO)
materials or other only	E33.038Comprising only Group IV-VI
impurities, Group IV element	compound (EPO)
(e.g., Si-SiGe superlattice) (EPO)	E33.039Comprising only Group II-IV- VI compound (EPO)
E33.01Doped superlattice (e.g., nipi superlattice) (EPO)	E33.04Comprising only Group I-III-
E33.011For current confinement (EPO)	VI compound (EPO) E33.041Characterized by doping
E33.012Multiple active regions between two electrodes (e.g.,	material (EPO)
stacks) (EPO)	E33.042Comprising only Group IV-VI or II-IV-VI compound (EPO)
E33.013 Material of active region (EPO)	E33.043Physical imperfections (e.g.,
E33.014In different regions (EPO)	particular concentration or
E33.015Comprising only Group IV	distribution of impurity)
element (EPO) E33.016With heterojunction (EPO)	(EPO)
133.010with necetojanecton (EFO)	

E33.044	.Device characterized by their operation (EPO)	E33.073Refractive means (e.g., lens) (EPO)
E33.045	Having p-n or hi-lo junction (EPO)	E33.074Scattering means (e.g., surface roughening) (EPO)
E33.046	P-I-N device (EPO)	E33.075 With means for cooling or
E33.047	Having at least two p-n	heating (EPO)
	junctions (EPO)	E33.076With means for light detecting
E33.048	Having heterojunction or graded	(e.g., photodetector) (EPO)
	gap (EPO)	E33.077 Monolithic integration with
E33.049	Comprising only Group III-V	photosensitive device (EPO)
⊞22 OF	compound (EPO)	E31.001 SEMICONDUCTOR DEVICES RESPONSIVE OR SENSITIVE TO
E33.05	Comprising only Group II-IV compound (EPO)	ELECTROMAGNETIC RADIATION
F33 051	Having Schottky barrier (EPO)	(E.G., INFRARED RADIATION,
	Having MIS barrier layer (EPO)	ADAPTED FOR CONVERSION OF
	Characterized by field-effect	RADIATION INTO ELECTRICAL
133.033	operation (EPO)	ENERGY OR FOR CONTROL OF
E33.054	Device being superluminescent	ELECTRICAL ENERGY BY SUCH
	diode (EPO)	RADIATION PROCESSES, OR
E33.055	.Detail of nonsemiconductor	APPARATUS PECULIAR TO
	component other than light-	MANUFACTURE OR TREATMENT OF
	emitting semiconductor device	SUCH DEVICES, OR OF PARTS THEREOF) (EPO)
	(EPO)	E31.002 .Characterized by semiconductor
	Packaging (EPO)	body (EPO)
E33.057	Adapted for surface mounting	E31.003Characterized by semiconductor
₽22 OE0	(EPO)	body material (EPO)
	Housing (EPO)Encapsulation (EPO)	E31.004Inorganic materials (EPO)
	Coatings (EPO)	E31.005 In different semiconductor
	Comprising luminescent	regions (e.g., Cu 2 X/CdX
шээ.оот	material (e.g., fluorescent)	heterojunction and X being
	(EPO)	Group VI element) (EPO)
E33.062	Electrodes (EPO)	E31.006Comprising only Cu 2 X/CdX
E33.063	Characterized by material	heterojunction and X being Group VI element (EPO)
	(EPO)	E31.007Comprising only
E33.064	Comprising transparent	heterojunction including Group
	conductive layers (e.g.,	I-III-VI compound (e.g., CdS/
	transparent conductive oxides	CuInSe 2 heterojunction) (EPO)
	(TCO), indium tin oxide (ITO)) (EPO)	E31.008Selenium or tellurium (EPO)
E33.065	Characterized by shape (EPO)	E31.009For device having potential
	Electrical contact or lead	or surface barrier (EPO)
	(e.g., lead frame) (EPO)	E31.01Characterized by doping
E33.067	Means for light extraction or	material (EPO)
	guiding (EPO)	E31.011Including, apart from doping
E33.068	Integrated with device (e.g.,	<pre>material or other impurity, only Group IV element (EPO)</pre>
	back surface reflector, lens)	E31.012For device having potential
	(EPO)	or surface barrier (EPO)
E33.069	Comprising resonant cavity	E31.013Comprising porous silicon as
	structure (e.g., Bragg	part of active layer (EPO)
₽22 <u>0</u> 7	reflector pair) (EPO)	E31.014Characterized by doping
	Comprising window layer (EPO)	material (EPO)
1/ U . C C ت	Not integrated with device (EPO)	
E33.072	Reflective means (EPO)	

257 - 24 CLASS 257 ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID-STATE DIODES)

E31.015Including, apart from doping material or other impurity, only Group II-VI compound (e.g., CdS, ZnS, HgCdTe) (EPO)	E31.035Including, apart from doping material or other impurity, only Group IV element or compound (e.g., Si-SiGe
E31.016For device having potential	superlattice) (EPO)
or surface barrier (EPO)	E31.036Doping superlattice (e.g.,
E31.017Characterized by doping	nipi superlattice) (EPO)
material (EPO)	E31.037For device having potential or
E31.018Including ternary compound	surface barrier (EPO)
(e.g., HgCdTe) (EPO)	E31.038Shape of body (EPO)
E31.019Including, apart from doping material or other impurity,	E31.039Shape of potential or surface barrier (EPO)
only Group III-V compound	E31.04Characterized by semiconductor
(EPO)	body crystalline structure or
E31.02For device having potential	plane (EPO)
or surface barrier (EPO)	E31.041 Including thin film deposited
E31.021Characterized by doping	on metallic or insulating
material GaAlAs, InGaAs,	substrate (EPO)
InGaAsP (EPO)	E31.042Including only Group IV
E31.022Including ternary or	element (EPO)
quaternary compound (EPO)	E31.043Including polycrystalline
E31.023Including, apart from doping	semiconductor (EPO)
material or other impurity,	E31.044Including only Group IV
only Group IV compound (e.g.,	element (EPO)
SiC) (EPO)	E31.045Including microcrystalline
E31.024For device having potential	silicon (c-Si) (EPO)
or surface barrier (EPO)	E31.046Including microcrystalline
E31.025Characterized by doping material (EPO)	Group IV compound (e.g., c- SiGe, c-SiC) (EPO)
E31.026Including, apart from doping material or other impurity,	E31.047Including amorphous semiconductor (EPO)
only compound other than Group	E31.048Including only Group IV
II-VI, III-V, and IV compound	element (EPO)
(EPO)	E31.049Including Group IV compound
E31.027Comprising only Group I-III-	(e.g., SiGe, SiC) (EPO)
VI chalcopyrite compound	E31.05Having light-induced
(e.g., CuInSe 2 , CuGaSe 2 ,	characteristic variation
CuInGaSe 2) (EPO)	(e.g., Staebler-Wronski
E31.028Characterized by doping	effect) (EPO)
material (EPO)	E31.051Including other
E31.029Comprising only Group IV-VI	nonmonocrystalline material
or II-IV-VI chalcogenide	(e.g., semiconductor particles
compound (e.g., PbSnTe) (EPO)	embedded in insulating
E31.03Characterized by doping	material) (EPO)
material (EPO)	E31.052 .Adapted to control current flow
E31.031Characterized by doping	through device (e.g.,
material (EPO)	photoresistor) (EPO)
E31.032 Characterized by semiconductor	E31.053 For device having potential or
body shape, relative size, or	surface barrier (e.g.,
disposition of semiconductor	phototransistor) (EPO)
regions (EPO)	E31.054Device sensitive to infrared,
E31.033Multiple quantum well	visible, or ultraviolet
structure (EPO)	radiation (EPO)
E31.034Characterized by amorphous	

semiconductor layer (EPO)

E31.055	Characterized by only one	E31.079	Field-effect
	<pre>potential or surface barrier (EPO)</pre>	E31.08	<pre>phototransistor (EPO)With PN heterojunction gate</pre>
	Potential barrier being of point contact type (EPO)	E31.081	(EPO)Charge-coupled device (CCD)
	PN homojunction potential barrier (EPO)		(EPO)
E31.058	Device comprising active		<pre>Field-effect phototransistor (EPO)</pre>
	layer formed only by Group II- VI compound (e.g., HgCdTe IR	E31.083	Conductor-insulator- semiconductor type (EPO)
₽ 21 050	<pre>photodiode) (EPO)Device comprising active</pre>	E31.084	Diode or charge-coupled
E31.039	layer formed only by Group	E31.085	<pre>device (CCD) (EPO)Metal-insulator-</pre>
E31.06	<pre>III-V compound (EPO)Device comprising active</pre>		<pre>semiconductor field-effect transistor (EPO)</pre>
	layer formed only by Group IV compound (EPO)	E31.086	Device sensitive to very short
	PIN potential barrier (EPO)		<pre>wavelength (e.g., X-ray, gamma-ray, or corpuscular</pre>
E31.062	Device comprising Group IV amorphous material (EPO)	E31.087	radiation) (EPO)Bulk-effect radiation
E31.063	<pre>Potential barrier working in avalanche mode (e.g., avalanche photodiode) (EPO)</pre>		<pre>detector (e.g., Ge-Li compensated PIN gamma-ray detector) (EPO)</pre>
E31.064	Heterostructure (e.g.,	E31.088	Li-compensated PIN gamma-ray
	<pre>surface absorption or multiplication (SAM) layer) (EPO)</pre>	E31.089	<pre>detector (EPO)With surface barrier or shallow PN junction (e.g.,</pre>
E31.065	Schottky potential barrier (EPO)		<pre>surface barrier alpha-particle detector) (EPO)</pre>
E31.066	Metal-semiconductor-metal (MSM) Schottky barrier (EPO)	E31.09	With shallow PN junction (EPO)
E31.067	PN heterojunction potential barrier (EPO)	E31.091	Field-effect type (e.g., MIS- type detector) (EPO)
E31.068	Characterized by two potential or surface barriers (EPO)	E31.092	Device being sensitive to very short wavelength (e.g., X-ray, gamma-ray) (EPO)
E31.069	Bipolar phototransistor (EPO)	E31.093	Device sensitive to infrared, visible, or ultraviolet
E31.07	Characterized by at least	E21 004	radiation (EPO)
E31.071	three potential barriers (EPO)Photothyristor (EPO)		Comprising amorphous semiconductor (EPO)
E31.072	<pre>Static induction type (i.e., SIT device) (EPO)</pre>	E31.095	.Structurally associated with electric light source (e.g.,
E31.073	Field-effect type (e.g., junction field-effect		<pre>electroluminescent light source) (EPO)</pre>
E21 074	phototransistor) (EPO)	E31.096	Hybrid device containing photosensitive and
	With Schottky gate (EPO)Charge-coupled device (CCD) (EPO)		electroluminescent components within one single body (EPO)
E31.076	Photo MESFET (EPO)	E31.097	Light source controlled by
E31.077	With PN homojunction gate (EPO)		radiation-sensitive semiconductor device (e.g.,
E31.078	Charge-coupled device (CCD) (EPO)		<pre>image converter, image amplifier, image storage device) (EPO)</pre>

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E31.098Device without potential or	E31.115Position-sensitive and
surface barrier (EPO)	lateral-effect photodetector
E31.099Light source being	<pre>(e.g., quadrant photodiode)</pre>
semiconductor device with	(EPO)
potential or surface barrier	E31.116Device working in avalanche
<pre>(e.g., light-emitting diode)</pre>	mode (EPO)
(EPO)	E31.117 Encapsulation (EPO)
E31.1Device with potential or	E31.118For device having potential or
surface barrier (EPO)	surface barrier (EPO)
E31.101Semiconductor light source and	E31.119 Coatings (EPO)
radiation-sensitive	E31.12For device having potential or
semiconductor device both	surface barrier (EPO)
having potential or surface barrier (EPO)	E31.121For filtering or shielding
E31.102Formed in or on common	light (e.g., multicolor filter
substrate (EPO)	for photodetector) (EPO)
E31.103Radiation-sensitive	E31.122For shielding light (e.g., light-blocking layer, cold
semiconductor device	shield for infrared detector)
controlled by light source	(EPO)
(EPO)	E31.123For interference filter
E31.104Radiation-sensitive	(e.g., multilayer dielectric
semiconductor device without	filter) (EPO)
potential or surface barrier	E31.124 Electrode (EPO)
(e.g., photoresistor) (EPO)	E31.125For device having potential or
E31.105Light source being	surface barrier (EPO)
semiconductor device having	E31.126Transparent conductive layer
potential or surface barrier	(e.g., transparent conductive
<pre>(e.g., light-emitting diode)</pre>	oxide (TCO), indium tin oxide
(EPO)	(ITO) layer) (EPO)
E31.106Optical potentiometer (EPO)	E31.127Optical element associated with
E31.107Radiation-sensitive	device (EPO)
semiconductor device with	E31.128Device having potential or
<pre>potential or surface barrier (EPO)</pre>	surface barrier (EPO)
E31.108Semiconductor light source and	E31.129 Comprising luminescent member
radiation-sensitive	(e.g., fluorescent sheet)
semiconductor device both	(EPO)
having potential or surface	E31.13Texturized surface (EPO)
barrier (EPO)	E31.131Arrangement for temperature
E31.109Formed in or on common	regulation (e.g., cooling,
substrate (EPO)	heating, or ventilating) (EPO)
E31.11 .Detail of nonsemiconductor	E27.001 DEVICE CONSISTING OF A PLURALITY
component of radiation-	OF SEMICONDUCTOR OR OTHER
sensitive semiconductor device	SOLID STATE COMPONENTS FORMED IN OR ON A COMMON SUBSTRATE,
(EPO)	E.G., INTEGRATED CIRCUIT
E31.111 Input/output circuit of device	DEVICE (EPO)
(EPO)	E27.002 .Including bulk negative
E31.112For device having potential or	resistance effect component
surface barrier (EPO)	(EPO)
E31.113Circuit arrangement of general	E27.003Including Gunn-effect device
character for device (EPO)	(EPO)
E31.114For device having potential or	

E31.114 ...For device having potential or surface barrier (EPO)

E27.004 .Including solid state component for rectifying, amplifying, or switching without a potential barrier or surface barrier	E27.021Vertical bipolar transistor in combination with resistor or capacitor only (EPO)
(EPO)	E27.022Vertical bipolar
E27.005 .Including component using galvano-magnetic effects, e.g.	transistor in combination with diode only (EPO)
Hall effect (EPO)	E27.023Lateral bipolar transistor
E27.006 .Including piezo-electric,	in combination with diode,
electro-resistive, or magneto-	capacitor, or resistor (EPO)
resistive component (EPO)	E27.024Including combination of
E27.007 .Including superconducting	diode, capacitor, or resistor
component (EPO)	(EPO)
E27.008 .Including thermo-electric or thermo-magnetic component with or without a junction of	E27.025Including combination of capacitor or resistor only (EPO)
dissimilar material or thermo-	E27.026Integrated circuit having a
magnetic component (EPO)	three-dimensional layout (EPO)
E27.009 .Including semiconductor	E27.027Including components formed
component with at least one potential barrier or surface	on opposite sides of a semiconductor substrate (EPO)
barrier adapted for	E27.028Including component having an
rectifying, oscillating,	active region in common (EPO)
amplifying, or switching, or	E27.029Including component of the
Including integrated passive	field-effect type (EPO)
circuit elements (EPO)	E27.03In combination with bipolar
E27.01With semiconductor substrate	transistor and diode,
only (EPO)	capacitor, or resistor (EPO)
E27.011Including a plurality of	E27.031In combination with
components in a non-repetitive	vertical bipolar transistor
configuration (EPO)	and diode, capacitor, or
E27.012Made of compound	resistor (EPO)
semiconductor material, e.g.	E27.032In combination with
III-V material (EPO)	lateral bipolar transistor and
E27.013Integrated circuit having a	diode, capacitor, or resistor
two-dimensional layout of	(EPO)
components without a common	E27.033In combination with diode,
active region (EPO)	capacitor, or resistor (EPO)
E27.014Including a field-effect	E27.034In combination with
type component (EPO)	capacitor only (EPO)
E27.015In combination with bipolar	E27.035In combination with
transistor (EPO)	resistor only (EPO)
E27.016In combination with diode,	E27.036With component other than
resistor, or capacitor (EPO)	field-effect type (EPO)
E27.017In combination with bipolar	E27.037Bipolar transistor in
transistor and diode,	combination with diode,
resistor, or capacitor (EPO)	•
E27.018With component other than	capacitor, or resistor (EPO) E27.038Vertical bipolar
field-effect type (EPO)	
E27.019Bipolar transistor in	transistor in combination with
combination with diode,	diode, capacitor, or resistor
capacitor, or resistor (EPO)	(EPO)
E27.02Vertical bipolar	E27.039Vertical bipolar
transistor in combination with	transistor in combination with
diode capacitor or resistor	diode only (EPO)

diode, capacitor, or resistor

(EPO)

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E27.04	With Schottky diode only (EPO)	E27.063Means for preventing parasitic bipolar action	
E27.041	Vertical bipolar transistor in combination with resistor only (EPO)	between the different transistor regions, e.g latch-up prevention (EP	۲.
E27.042	Vertical bipolar transistor in combination with capacitor only (EPO)	E27.064Combination of complementary transisto having a different stru	ors
E27.043	Lateral bipolar transistor in combination with diode, capacitor, or resistor (EPO)	e.g. stacked CMOS, high voltage and low-voltage (EPO)	
E27.044	<pre>Including combination of diode, capacitor, or resistor (EPO)</pre>	in the substrate (EPO) E27.066Including a P-well	
	<pre>Combination of capacitor and resistor (EPO)</pre>	the substrate (EPO) E27.067Including both N- α	
E27.046	Including only semiconductor components of a single kind,	wells in the substrate, twin-tub (EPO)	
-05 045	e.g., all bipolar transistors, all diodes, or all CMOS (EPO)	E27.068Schottky barrier gate effect transistor (EPO)	
	Resistor only (EPO)Capacitor only (EPO)	E27.069PN junction gate fiel effect transistor	La-
	Varactor diode (EPO)	E27.07Including a plurality of	
E27.05	Metal-insulated- semiconductor (MIS) diode	individual components i repetitive configuratio E27.071Including resistor or	
E27.051	(EPO)Diode only (EPO)	capacitor only (EPO)	
E27.052	Thyristor only (EPO)Bipolar component only (EPO)	E27.072Including bipolar comp (EPO)	onent
E27.054	<pre>Combination of lateral and vertical transistors only (EPO)</pre>	E27.073Including diode only E27.074Including bipolar trans (EPO)	
E27.055	Vertical bipolar transistor only (EPO)	E27.075Bipolar dynamic rand access memory structure	
E27.056	Vertical direct transistor of the same conductivity type having different	E27.076Array of single bipo transistors only, e.g. only memory structure (read
	characteristics, (e.g. Darlington transistor) (EPO)	E27.077Static bipolar memor structure (EPO)	ry cell
	Vertical complementary transistor (EPO)	E27.078Bipolar electrically programmable memory str	
E27.058	<pre>Combination of direct and inverse vertical transistors (e.g., collector acts as</pre>	(EPO) E27.079Thyristor (EPO) E27.08Unijunction transisto	or,
	<pre>emitter) (EPO)Including field-effect component only (EPO)</pre>	i.e., three terminal de with only one p-n junct having a negative resis	ion
E27.06	<pre>Field-effect transistor with insulated gate (EPO)</pre>	region in the I-V characteristic (EPO)	
E27.061	Combination of depletion and enhancement field-effect	E27.081Including field-effect component (EPO)	
E27.062	transistors (EPO)Complementary MIS (EPO)	E27.082Including bucket brig type charge coupled dev (C.C.D) (EPO)	

E27.083	<pre>Including charge coupled device (C.C.D) or charge injection device (C.I.D) (EPO)</pre>	E27.111	Substrate comprising other than a semiconductor material, e.g. insulating substrate or
E27.084	Dynamic random access memory, DRAM, structure (EPO)		layered substrate Including a non-semiconductor layer (EPO)
E27.085	One-transistor memory cell	E27.112	Including insulator on
	structure, i.e., each memory cell containing only one		semiconductor, e.g. SOI (silicon on insulator) (EPO)
	transistor (EPO)	E27.113	Combined with thin-film or
E27.086	Storage electrode stacked over the transistor		thick-film passive component (EPO)
E27.087	With bit line higher than	E27.114	.Including only passive thin-film
F27 088	capacitor (EPO)With capacitor higher		or thick-film elements on a common insulating substrate
EZ7.000	than bit line level (EPO)		(EPO)
E27.089	Storage electrode having	E27.115	Thick-film circuits (EPO)
	multiple wings (EPO)		Thin-film circuits (EPO)
E27.09	<pre>Capacitor extending under the transistor (EPO)</pre>		.Including organic material in active region
	Transistor in trench (EPO)	E27.118	Including semiconductor
	Capacitor in trench (EPO)		components sensitive to infrared radiation, light, or
E27.093	Capacitor extending under		electromagnetic radiation of a
F27 N94	or around the transistor (EPO)Having storage electrode		shorter wavelength (EPO)
E27.074	extension stacked over the	E27.119	Including semiconductor
	transistor (EPO)		components with at least one
E27.095	Capacitor and transistor		potential barrier, surface
	in common trench (EPO)		barrier, or recombination zone adapted for light emission
	Vertical transistor (EPO)		(EPO)
	Peripheral structure (EPO)	E27.12	.Including semiconductor
	Static random access memory, SRAM, structure (EPO)		component with at least one potential barrier or surface
	Load element being a MOSFET transistor (EPO)		barrier adapted for light emission structurally
E27.1	Load element being a thin film transistor (EPO)		associated with controlling devices having a variable
E27.101	Load element being a resistor (EPO)		impedance and not being light
E27 102	Read-only memory, ROM,	DOT 101	sensitive (EPO)
227.102	structure (EPO)	E2/.121	In a repetitive configuration (EPO)
	Electrically programmable ROM (EPO)	E27.122	.Including active semiconductor component sensitive to
E27.104	Ferroelectric non-volatile		infrared radiation, light, or
TOF 105	memory structure (EPO)		electromagnetic radiation of a
	<pre>Masterslice integrated circuit (EPO)</pre>	E27.123	<pre>shorter wavelength (EPO)Energy conversion device (EPO)</pre>
E27.106	<pre>Using bipolar structure (EPO)</pre>	E27.124	In a repetitive configuration, e.g. planar multi-junction
E27.107	Using field-effect structure		solar cells (EPO)
DOT 100	(EPO)	E27.125	Including only thin film
	CMOS gate array (EPO)		solar cells deposited on a
r∠/.109	<pre>Using combined field-effect/ bipolar structure (EPO)</pre>		substrate (EPO)
E27.11	<pre>Input and output buffer/ driver (EPO)</pre>		

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T07 106		T07 147 C
EZ/.126	Including multiple vertical	E27.147Contact-type imager (e.g.,
	junction or V-groove junction	contacts document surface)
	solar cells formed in a	(EPO)
	semiconductor substrate (EPO)	E27.148Junction field effect
E27.127	Device controlled by radiation	transistor (JFET) imager or
	(EPO)	static induction transistor
E27.128	With at least one potential	(SIT) imager (EPO)
	barrier or surface barrier	E27.149Bipolar transistor imager
	(EPO)	(EPO)
E27.129	In a repetitive configuration	E27.15Charge coupled imager (EPO)
	(EPO)	E27.151Structural or functional
E27.13	Imager Including structural or	details (EPO)
	functional details of the	E27.152Geometry or disposition of
	device (EPO)	pixel-elements, address lines
E27.131	Geometry or disposition of	or gate-electrodes (EPO)
	pixel-elements, address-lines,	E27.153Linear CCD imager (EPO)
	or gate-electrodes (EPO)	E27.154Area CCD imager (EPO)
E27.132	Pixel-elements with	E27.155Frame-interline transfer
	integrated switching, control,	(EPO)
	storage, or amplification	E27.156Interline transfer (EPO)
	elements (EPO)	E27.150Frame transfer (EPO)
E27 133	Photodiode array or MOS	
127.133	imager (EPO)	E27.158Charge injection device
F27 134	Color imager (EPO)	(CID) imager (EPO)
	Multicolor imager having a	E27.159CCD or CID color imager
EZ/.133		(EPO)
	stacked pixel-element	E27.16Infrared CCD or CID imager
	structure, e.g. npn, npnpn or MQW elements (EPO)	(EPO)
E27 126		$E27.161 \dots Of$ the hybrid type (e.g.,
	Infrared imager (EPO)	chip-on-chip, bonded
E27.137	Of the hybrid type (e.g.,	substrates) (EPO)
	chip-on-chip, bonded	E27.162Anti-blooming (EPO)
TOT 120	substrates) (EPO)	E27.163Including a photoconductive
E27.138	Multispectral infrared	layer deposited on the CCD
	imager having a stacked pixel-	structure (EPO)
	element structure, e.g., npn,	E29.001 SEMICONDUCTORS DEVICES ADAPTED
-05 100	npnpn or MQW structures (EPO)	FOR RECTIFYING, AMPLIFYING,
	Anti-blooming (EPO)	OSCILLATING, OR SWITCHING,
E27.14	X-ray, gamma-ray, or high	CAPACITORS, OR RESISTORS WITH
	energy radiation imager	AT LEAST ONE POTENTIAL-JUMP
	(measuring X-, gamma- or	BARRIER OR SURFACE BARRIER
	corpuscular radiation) (EPO)	(EPO)
E27.141	Imager using a photoconductor	E29.002 .Electrical characteristics due
	layer (e.g., single	to properties of entire
	photoconductor layer for all	semiconductor body rather than
	pixels) (EPO)	just surface region (EPO)
	Color imager (EPO)	E29.003Characterized by their
	Infrared imager (EPO)	crystalline structure (e.g.,
E27.144	Of the hybrid type (e.g.,	polycrystalline, cubic)
	chip-on-chip, bonded	particular orientation of
	substrates) (EPO)	crystalline planes (EPO)
E27.145	Anti-blooming (EPO)	E29.004With specified crystalline
E27.146	\ldots X-ray, gamma-ray, or high	planes or axis (EPO)
	energy radiation imagers (EPO)	

E29.005Characterized by specified shape or size of PN junction or by specified impurity concentration gradient within	E29.017With field relief electrodes acting on insulator potential or insulator charges (EPO)
the device (EPO) E29.006Characterized by particular design considerations to	E29.018Comprising internal isolation within devices or components (EPO)
control electrical field effect within device (EPO)	E29.019Isolation by PN junctions (EPO)
E29.007For controlling surface leakage or electric field	E29.02Isolation by dielectric regions (EPO)
concentration (EPO) E29.008For controlling breakdown	E29.021For source or drain region of field-effect device (EPO)
voltage of reverse biased devices (EPO)	E29.022Characterized by shape of semiconductor body (EPO)
E29.009With field relief electrode (field plate) (EPO)	E29.023Adapted for altering junction breakdown voltage by shape of
E29.01With at least two field relief electrodes used in	semiconductor body (EPO) E29.024Characterized by shape,
combination and not electrically interconnected (EPO)	relative sizes or dispositions of semiconductor regions or junctions between regions
E29.011With one or more field	(EPO)
relief electrode comprising resistance material (e.g., semi insulating material,	E29.025Characterized by particular shape of junction between semiconductor regions (EPO)
lightly doped poly-silicon) (EPO)	E29.026Surface layout of device (EPO)
E29.012By doping profile or shape or arrangement of the PN junction, or with	E29.027Surface layout of MOS gated device (e.g., DMOSFET or IGBT) (EPO)
supplementary regions (e.g., guard ring, LDD, drift region)	E29.028With a nonplanar gate structure (EPO)
(EPO) E29.013With supplementary region doped oppositely to or in rectifying contact with semiconductor containing or contacting region(e.g., guard rings with PN or Schottky junction) (EPO)	E29.029With semiconductor regions connected to electrode carrying current to be rectified, amplified or switched and such electrode being part of semiconductor device which comprises three or more electrodes (EPO)
E29.014With breakdown supporting region for localizing breakdown or limiting its	E29.03Emitter regions of bipolar transistors (EPO)
voltage (EPO) E29.015With insulating layer	E29.031Of lateral transistors (EPO) E29.032Noninterconnected
characterized by dielectric or electrostatic property (e.g.,	multiemitter structures (EPO) E29.033Of heterojunction bipolar transistors (EPO)
<pre>including fixed charge or semi-insulating surface layer) (EPO)</pre>	E29.034Collector regions of bipolar transistors (EPO)
E29.016For preventing surface leakage due to surface inversion layer (e.g., channel stop) (EPO)	E29.035Pedestal collectors (EPO) E29.036Anode or cathode regions of thyristors or gated bipolar- mode devices (EPO)

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E29.037	Anode regions of thyristors or gated bipolar-mode devices		With insulated gate (EPO)
E29.038	(EPO)Cathode regions of		<pre>supplementary region (e.g., for preventing punch-through,</pre>
E29.039	thyristors (EPO)Source or drain regions of field-effect devices (EPO)	F29 064	<pre>improving capacity effect or leakage current) (EPO) Characterized by contact</pre>
E29.04	Of field-effect transistors with insulated gate (EPO)	E27.004	structure of substrate region (EPO)
	Of field-effect transistors with Schottky gate (EPO)		<pre>Of charge coupled devices (EPO)</pre>
	Tunneling barrier (EPO)With semiconductor regions connected to electrode not carrying current to be	E29.066	Body region structure of IGFET's with channel containing layer (DMOSFET or IGBT) (EPO)
	rectified, amplified or switched and such electrode	E29.067	With nonplanar gate structure (EPO)
	being part of semiconductor device which comprises three		Characterized by materials of semiconductor body (EPO)
E29.044	or more electrodes (EPO)Base region of bipolar		Single quantum well structures (EPO)
	transistors (EPO)		Quantum wire structures (EPO)
	Of lateral transistors (EPO)	E29.071	Quantum box or quantum dot
E29.046	Base regions of thyristors (EPO)	E20 072	structures (EPO)
E29.047	Anode base regions of thyristors (EPO)	E29.072	<pre>Structures with periodic or quasi-periodic potential variation, (e.g., multiple</pre>
E29.048	Cathode base regions of thyristors (EPO)		quantum wells, superlattices) (EPO)
E29.049	Channel region of field- effect devices (EPO)	E29.073	Doping structures (e.g., doping superlattices, nipi-
E29.05	<pre>Of field-effect transistors (EPO)</pre>	E29.074	<pre>superlattices) (EPO)Structures without potential</pre>
	With insulated gate (EPO)		periodicity in direction
	Nonplanar channel (EPO)		perpendicular to major surface of substrate (e.g., lateral
E29.053	With nonuniform doping structure in channel region		superlattice) (EPO)
T20 0F4	surface (EPO)	E29.075	Compositional structures (EPO)
E29.054	Doping structure being parallel to channel length	E29.076	With layered structures with
	(EPO)		quantum effects in vertical
E29.055	With vertical doping		direction (EPO)
	variation (EPO)	E29.077	Comprising at least one
E29.056	With variation of composition of channel (EPO)		<pre>long-range structurally disordered material (e.g.,</pre>
E29.057	With PN junction gate		one-dimensional vertical
E29.058	Of charge coupled devices	F29 078	amorphous superlattices) (EPO)Comprising only
-00 050	(EPO)	E29.070	semiconductor materials (EPO)
E29.059	Gate region of field-effect devices with PN junction gate (EPO)	E29.079	Two or more elements from two or more groups of Periodic
E29.06	Substrate region of field-		Table of elements (e.g., alloys) (EPO)
E29.061	<pre>effect devices (EPO)Of field-effect transistors (EPO)</pre>	E29.08	Amorphous materials (EPO)

E29.081	In different semiconductor regions (e.g.,	E29.105	Characterized by combinations of two or more features of
	heterojunctions) (EPO)Only element from fourth group of Periodic System in uncombined form (EPO)Amorphous materials (EPO)		crystalline structure, shape, materials, physical imperfections, and concentration/distribution of impurities in bulk material
	Including two or more of elements from fourth group of Periodic System (EPO)	E29.106	<pre>(EPO)Characterized by physical imperfections; having polished</pre>
E29.085	<pre>In different semiconductor regions (e.g., heterojunctions) (EPO)</pre>	E29.107	or roughened surface (EPO)Imperfections within semiconductor body (EPO)
E29.086	Further characterized by doping material (EPO)	E29.108	Imperfections on surface of semiconductor body (EPO)
	Selenium or tellurium only (EPO)	E29.109	Characterized by concentration or distribution of impurities
	Amorphous materials (EPO)	TOO 11	in bulk material (EPO)
	Only Group III-V compounds (EPO)	E29.11	Planar doping (e.g., atomic- plane doping, delta-doping) (EPO)
E29.09	Including two or more compounds (e.g., alloys) (EPO)	E29.111	.Electrodes (EPO)
F29 N91	In different semiconductor		Characterized by their shape,
127.071	regions (e.g., heterojunctions) (EPO)		relative sizes or dispositions (EPO)
E29.092	Amorphous materials (EPO)	E29.113	Carrying current to be
	Further characterized by doping material (EPO)		rectified, amplified or switched (EPO)
E29.094	Only Group II-VI compounds	E29.114	Emitter or collector
	(EPO)		electrodes for bipolar
	Amorphous materials (EPO)	₽20 11E	transistors (EPO)Cathode or anode electrodes
E29.096	Including two or more	E29.113	for thyristors (EPO)
-00 000	compounds (e.g., alloys) (EPO)	E29.116	Source or drain electrodes
E29.097	In different semiconductor	,	for field-effect devices (EPO)
	regions (e.g.,	E29.117	For thin film transistors
F20 008	heterojunctions) (EPO)Further characterized by		with insulated gate (EPO)
	doping material (EPO)	E29.118	For vertical current flow
E29.099	CdX compounds being one	E20 110	(EPO)For lateral devices where
	element of sixth group of	E29.119	connection to source or drain
E29.1	Periodic System (EPO)Semiconductor materials other than Group IV, selenium, tellurium, or Group III-V		region is done through at least one part of semiconductor substrate
	compounds (EPO)		thickness (e.g., with connecting sink or with via-
	Amorphous materials (EPO)		hole) (EPO)
E29.102	Group I-VI or I-VII compounds	E29.12	Layout configuration for
E29.103	(e.g., Cu 2 O, CuI) (EPO)Pb compounds (e.g., PbO)		lateral device source or drain region (e.g., cellular,
TO 104	(EPO)		interdigitated or ring
E29.1U4	Si compounds (e.g., SiC) (EPO)		structure or being curved or angular) (EPO)
		E29.121	Source or drain electrode in groove (EPO)

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T00 100	T00 140
E29.122Characterized by relative	E29.148Schottky barrier electrodes
position of source or drain electrode and gate electrode	(EPO) E29.149On Group III-V material (EPO)
(EPO)	E29.15Electrodes for IGFET (EPO)
E29.123Not carrying current to be	E29.15For TFT (EPO)
rectified, amplified, or	E29.151 With lateral structure (e.g.,
switched (EPO)	poly-silicon gate with lateral
E29.124Base electrodes for bipolar	doping variation or with
transistors (EPO)	lateral composition variation
E29.125Gate electrodes for	or characterized by sidewalls
thyristors (EPO)	being composed of conductive,
E29.126Gate stack for field-effect	resistivity) (EPO)
devices (EPO)	E29.154Silicon gate conductor
E29.127For field-effect transistors	material (EPO)
(EPO)	E29.155Multiple silicon layers
E29.128With insulated gate (EPO)	E29.156Including silicide layer
E29.129Gate electrodes for	contacting silicon layer (EPO)
transistors with floating gate	E29.157Including barrier layer
(EPO)	between silicon and non-Si
E29.13Gate electrodes for	electrode
nonplanar MOSFET (EPO)	E29.158Elemental metal gate
E29.131	conductor material (e.g., W,
regions at different vertical	Mo) (EPO)
level having channel composed	E29.159Diverse conductors (EPO)
only of vertical sidewall	E29.16Gate conductor material being
connecting drain and source layers (EPO)	compound or alloy material
E29.132Characterized by	(e.g., organic material, TiN, MoSi 2) (EPO)
insulating layer (EPO)	E29.161Silicide (EPO)
E29.133Nonuniform insulating	E29.162Insulating materials for
layer thickness (EPO)	IGFET (EPO)
E29.134Characterized by	E29.164With at least one
configuration of gate	ferroelectric layer (EPO)
electrode layer (EPO)	E29.165Multiple layers (EPO)
E29.135Characterized by length	E29.166 .Types of semiconductor device
or sectional shape (EPO)	(EPO)
E29.136Characterized by surface	E29.167Controllable by plural effects
lay-out (EPO)	that include variations in
E29.137Characterized by	magnetic field, mechanical
configuration of gate stack of	force, or electric current/
thin film FETs (EPO)	potential applied to device or one or more electrodes of
E29.138For charge coupled devices (EPO)	device (EPO)
E29.139Of specified material (EPO)	E29.168Quantum effect device (EPO)
E29.14For gate of heterojunction	E29.169Controllable by only signal
field-effect devices (EPO)	applied to control electrode
E29.141Resistive materials for field-	(e.g., base of bipolar
effect devices (EPO)	transistor, gate of field-
E29.142 Superconductor materials (EPO)	effect transistor) (EPO)
E29.143Ohmic electrodes (EPO)	E29.17Memory effect devices (EPO)
E29.144On Group III-V material (EPO)	E29.171Bipolar device (EPO)
E29.145On thin-film Group III-V	E29.172Double-base diode (EPO)
material (EPO)	E29.173Transistor-type device (i.e.,
E29.146On silicon (EPO)	able to continuously respond
E29.147For thin-film silicon (EPO)	to applied control signal)
/	

	Bipolar junction transistorStructurally associated	E29.196	(e.g., field-controlled
E29.176	<pre>with other devices (EPO)Device being resistive element (e.g., ballasting</pre>		thyristor (FCTh), static induction thyristor (SITh)) (EPO)
	resistor) (EPO)	E29.197	Insulated gate bipolar mode
E29.177	Point contact transistors (EPO)		<pre>transistor (e.g., IGBT; IGT; COMFET) (EPO)</pre>
E29.178	Schottky transistors (EPO)	E29.198	Transistor with vertical
	Tunnel transistors (EPO)		current flow (EPO)
	Avalanche transistors (EPO)	E29.199	With both emitter and
E29.181	Transistors with hook collector (i.e., collector		<pre>collector contacts in same substrate side (EPO)</pre>
	having two layers of opposite	E29.2	With nonplanar surface
	conductivity type (e.g., SCR))		(e.g., with nonplanar gate or
	(EPO)		with trench or recess or
E29.182	Bipolar thin-film transistors (EPO)		pillar in surface of emitter, base, or collector region for
E29 183	Vertical transistor (EPO)		improving current density or
			short-circuiting emitter and
	base-collector junctions in		base regions) (EPO)
	same plane (EPO)	E29.201	And gate structure lying
E29.185	Having emitter-base		on slanted or vertical surface
	junction and base-collector		or formed in groove (e.g.,
	junction on different surfaces	E20 202	<pre>trench gate IGBT) (EPO)Thin-film device (EPO)</pre>
	(e.g., mesa planar transistor)		Thyristor-type device (e.g.,
E20 106	(EPO)	DD7.211	having four-zone regenerative
E29.186	Inverse vertical transistor (EPO)		action) (EPO)
F29 187	Lateral transistor (EPO)	E29.212	Gate-turn-off device (EPO)
	Hetero-junction transistor	E29.213	With turn off by field
	(EPO)	T00 014	effect (EPO)
	Vertical transistors (EPO)	E29.214	Produced by insulated gate structure (EPO)
E29.19	Having two-dimensional	E29 215	Bidirectional device (e.g.,
	<pre>base (e.g., modulation-doped base, inversion layer base,</pre>	227.213	triac) (EPO)
	delta-doped base) (EPO)	E29.216	With turn on by field effect
E29.191			(EPO)
	one or more nonmonocrystalline	E29.217	Combined structurally with
	elements of Group IV (e.g.,		at least one other device
	amorphous silicon) alloys	T00 010	(EPO)
	comprising Group IV elements	E29.218	Combined with capacitor or resistor (EPO)
₽20 102	(EPO)Resonant tunneling	E29 219	Combined with diode (EPO)
E27.172	transistors (EPO)		Antiparallel diode (EPO)
E29 193	Comprising lattice		Combined with field-effect
117.17 3	mismatched active layers		transistor (EPO)
	(e.g., SiGe strained layer	E29.222	Having built-in localized
	transistors) (EPO)		breakdown/breakover region
E29.194	Controlled by field effect		(EPO)
	(e.g., bipolar static	E29.223	Having amplifying gate
	<pre>induction transistor (BSIT)) (EPO)</pre>		<pre>structure (e.g., Darlington configuration) (EPO)</pre>
E29.195	Gated diode structure (EPO)	E29.224	Asymmetrical thyristor (EPO)
			Lateral thyristor (EPO)

257 - 36 CLASS 257 ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID-STATE DIODES)

E29.226Unipolar device (EPO)	E29.252With direct single
E29.227Charge transfer device (EPO)	heterostructure (i.e., with
E29.228Charge-coupled device (EPO)	wide bandgap layer formed on
E29.229With field effect produced	top of active layer (e.g.,
by insulated gate (EPO)	direct single heterostructure
E29.23Input structure (EPO)	MIS-like HEMT)) (EPO)
_	E29.253With wide bandgap charge-
E29.231Output structure (EPO)	carrier supplying layer (e.g.,
E29.232Structure for improving	direct single heterostructure
output signal (EPO)	MODFET) (EPO)
E29.233Buried channel CCD (EPO)	E29.254With delta-doped channel
E29.234Two-phase CCD (EPO)	(EPO)
E29.235Three-phase CCD (EPO)	E29.255With field effect produced
E29.236Four-phase CCD (EPO)	
E29.237Surface channel CCD (EPO)	by insulated gate (EPO)
E29.238Two-phase CCD (EPO)	E29.256With channel containing
E29.239Three-phase CCD (EPO)	layer contacting drain drift
E29.24Four-phase CCD (EPO)	region (e.g., DMOS transistor)
E29.241 Hot electron transistor (HET)	(EPO)
or metal base transistor (MBT)	E29.257Having vertical bulk
(EPO)	current component or current
E29.242Field-effect transistor (EPO)	vertically following trench
E29.243Using static field induced	gate (e.g., vertical power
region (e.g., SIT, PBT) (EPO)	DMOS transistor) (EPO)
E29.244Velocity modulations	E29.258With both source and
transistor (i.e., VMT) (EPO)	drain contacts in same
E29.245With one-dimensional charge	substrate side (EPO)
carrier gas channel (e.g.,	E29.259With nonplanar surface
quantum wire FET) (EPO)	(EPO)
E29.246With two-dimensional charge	E29.26Channel structure lying
carrier gas channel (e.g.,	under slanted or vertical
HEMT; with two-dimensional	surface or being formed along
	surface of groove (e.g.,
charge-carrier layer formed at	trench gate DMOSFET) (EPO)
heterojunction interface)	E29.261With at least part of
(EPO)	active region on insulating
E29.247With inverted single	substrate (e.g., lateral DMOS
heterostructure (i.e., with	in oxide isolated well) (EPO)
active layer formed on top of	E29.262Vertical transistor (EPO)
wide bandgap layer (e.g.,	E29.263Comprising gate-to-body
IHEMT)) (EPO)	connection (i.e., bulk dynamic
E29.248With confinement of	threshold voltage MOSFET)
carriers by at least two	(EPO)
heterojunctions (e.g., DHHEMT,	E29.264With multiple gate
quantum well HEMT, DHMODFET)	structure (EPO)
(EPO)	E29.265Structure comprising MOS
E29.249Using Group III-V	gate and at least one non-MOS
semiconductor material (EPO)	gate (e.g., JFET or MESFET
E29.25With more than one donor	gate) (EPO)
layer (EPO)	E29.266With lightly doped drain or
E29.251With delta or planar	source extension (EPO)
doped donor layer (EPO)	E29.267With nonplanar structure
	(e.g., gate or source or drain
	being nonplanar) (EPO)

E29.268Source region and drain region having nonsymmetrical structure about gate electrode	E29.292Polycrystalline or microcrystalline silicon transistor (EPO)
(EPO)	E29.293With top gate (EPO)
E29.269With overlap between	E29.294With inverted
lightly doped extension and	transistor structure (EPO)
gate electrode (EPO)	E29.295Characterized by
E29.27With buried channel (EPO)	insulating substrate or
E29.271With Schottky drain or	support (EPO)
source contact (EPO)	E29.296Comprising Group III-V or
E29.272Gate comprising	II-VI compound, or of Se, Te,
ferroelectric layer (EPO)	or oxide semiconductor (EPO)
E29.273Thin-film transistor (EPO)	E29.297Comprising Group IV non-Si
E29.274Vertical transistor (EPO)	semiconductor materials or
E29.275With multiple gates (EPO)	alloys (e.g., Ge, SiN alloy,
E29.276With supplementary region	SiC alloy) (EPO)
or layer in thin film or in	E29.298With multilayer structure
insulated bulk substrate	or superlattice structure
supporting it for controlling	(EPO)
or increasing voltage	E29.299Characterized by property
resistance of device (EPO)	or structure of channel or
E29.277Characterized by drain or	contact thereto (EPO)
source properties (EPO)	E29.3With floating gate (EPO)
E29.278With LDD structure or	E29.301Programmable by two single
extension or offset region or	electrons (EPO)
characterized by doping	E29.302Hi-lo programming levels
profile (EPO)	only (EPO)
E29.279Asymmetrical source and drain regions (EPO)	E29.303Charging by injection of carriers through conductive
E29.28For preventing leakage current (EPO)	<pre>insulator (e.g., Poole-Frankel conduction) (EPO)</pre>
E29.281For preventing kink or	E29.304
snapback effect (e.g.,	carriers (e.g., Fowler-
discharging minority carriers	Nordheim tunneling) (EPO)
of channel region for	E29.305Charging by hot carrier
preventing bipolar effect)	injection (EPO)
(EPO)	E29.306
E29.282With light shield (EPO)	from channel (EPO)
E29.283With supplementary region	E29.307
or layer for improving	avalanche breakdown of PN
flatness of device (EPO)	junction (e.g., FAMOS) (EPO)
E29.284With drain or source	E29.308Programmable with more
connected to bulk conducting	than two possible different
substrate (EPO)	levels (EPO)
E29.285Silicon transistor (EPO)	E29.309With charge trapping gate
E29.286Monocrystalline only (EPO)	<pre>insulator (e.g., MNOS-memory transistors) (EPO)</pre>
E29.287SOS transistor (EPO)	E29.31With field effect produced
E29.288Nonmonocrystalline (EPO)	by PN or other rectifying
E29.289Amorphous silicon	junction gate (i.e., potential
transistor (EPO)	barrier) (EPO)
E29.29With top gate (EPO)	E29.311With Schottky drain or
E29.291With inverted	source contact (EPO)
+	
transistor structure (EPO)	

257 - 38 CLASS 257 ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID-STATE DIODES)

E29.312With PN junction gate (e.g., PN homojunction gate) (EPO)	E29.337Thyristor diode (i.e., having only two terminals and no control electrode (e.g.,
E29.313Vertical transistors (EPO) E29.314Thin-film JFET (EPO)	Shockley diode, break-over diode)) (EPO)
E29.315With heterojunction gate	E29.338Schottky diode (EPO)
(e.g., transistors with	E29.339Tunneling diode (EPO)
semiconductor layer acting as	E29.34Resonant tunneling diode
gate insulating layer) (EPO)	(i.e., RTD, RTBD) (EPO)
E29.316Programmable transistor	E29.341Esaki diode (EPO)
(e.g., with charge-trapping	E29.342 Capacitor with potential
quantum well) (EPO)	barrier or surface barrier
E29.317With Schottky gate (EPO)	(EPO)
E29.318Vertical transistors (EPO)	E29.343Conductor-insulator-conductor
E29.319With multiple gate (EPO)	capacitor on semiconductor
E29.32Thin-film MESFET (EPO)	substrate (EPO)
E29.321With recessed gate (EPO)	E29.344Variable capacitance diode
E29.322Single electron transistors:	(e.g., varactors) (EPO)
Coulomb blockade device (EPO)	E29.345Metal-insulator-semiconductor
E29.323 Controllable by variation of	(e.g., MOS capacitor) (EPO)
magnetic field applied to	E29.346Trench capacitor (EPO)
device (EPO)	E29.347Controllable by thermal signal
E29.324Controllable by variation of	(e.g., IR) (EPO)
applied mechanical force	E45.001 SOLID-STATE DEVICES ADAPTED FOR
(e.g., of pressure) (EPO)	RECTIFYING, AMPLIFYING,
E29.325Controllable only by variation	OSCILLATING, OR SWITCHING
of electric current supplied	WITHOUT POTENTIAL-JUMP BARRIER
or only electric potential	OR SURFACE BARRIER, E.G.,
applied to alegtwode gazzring	DIFIECTRIC TRIODES ONSHINSKY-
applied to electrode carrying	DIELECTRIC TRIODES; OVSHINSKY-
current to be rectified,	EFFECT DEVICES, PROCESSES, OR
current to be rectified, amplified, oscillated, or	
current to be rectified, amplified, oscillated, or switched (EPO)	EFFECT DEVICES, PROCESSES, OR APPARATUS PECULIAR TO
current to be rectified, amplified, oscillated, or	EFFECT DEVICES, PROCESSES, OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT
current to be rectified, amplified, oscillated, or switched (EPO) E29.326Resistor with PN junction	EFFECT DEVICES, PROCESSES, OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT THEREOF, OR OF PARTS THEREOF
current to be rectified, amplified, oscillated, or switched (EPO) E29.326Resistor with PN junction (EPO) E29.327Diode (EPO)	EFFECT DEVICES, PROCESSES, OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT THEREOF, OR OF PARTS THEREOF (EPO)
current to be rectified, amplified, oscillated, or switched (EPO) E29.326Resistor with PN junction (EPO)	EFFECT DEVICES, PROCESSES, OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT THEREOF, OR OF PARTS THEREOF (EPO) E45.002 .Bistable switching devices, e.g., Ovshinsky-effect devices (EPO)
current to be rectified, amplified, oscillated, or switched (EPO) E29.326Resistor with PN junction (EPO) E29.327Diode (EPO) E29.328Planar PN junction diode	EFFECT DEVICES, PROCESSES, OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT THEREOF, OR OF PARTS THEREOF (EPO) E45.002 .Bistable switching devices, e.g., Ovshinsky-effect devices (EPO) E45.003Switching materials being
current to be rectified, amplified, oscillated, or switched (EPO) E29.326Resistor with PN junction (EPO) E29.327Diode (EPO) E29.328Planar PN junction diode (EPO)	EFFECT DEVICES, PROCESSES, OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT THEREOF, OR OF PARTS THEREOF (EPO) E45.002 .Bistable switching devices, e.g., Ovshinsky-effect devices (EPO) E45.003Switching materials being oxides or nitrides (EPO)
current to be rectified, amplified, oscillated, or switched (EPO) E29.326Resistor with PN junction (EPO) E29.327Diode (EPO) E29.328Planar PN junction diode (EPO) E29.329Mesa PN junction diode (EPO)	EFFECT DEVICES, PROCESSES, OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT THEREOF, OR OF PARTS THEREOF (EPO) E45.002 .Bistable switching devices, e.g., Ovshinsky-effect devices (EPO) E45.003Switching materials being oxides or nitrides (EPO) E45.004N: Light-controlled Ovshinsky
current to be rectified, amplified, oscillated, or switched (EPO) E29.326Resistor with PN junction (EPO) E29.327Diode (EPO) E29.328Planar PN junction diode (EPO) E29.329Mesa PN junction diode (EPO) E29.33Hi-lo semiconductor device	EFFECT DEVICES, PROCESSES, OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT THEREOF, OR OF PARTS THEREOF (EPO) E45.002 .Bistable switching devices, e.g., Ovshinsky-effect devices (EPO) E45.003Switching materials being oxides or nitrides (EPO) E45.004N: Light-controlled Ovshinsky devices (EPO)
current to be rectified, amplified, oscillated, or switched (EPO) E29.326Resistor with PN junction (EPO) E29.327Diode (EPO) E29.328Planar PN junction diode (EPO) E29.329Mesa PN junction diode (EPO) E29.33Hi-lo semiconductor device (e.g., memory device) (EPO)	EFFECT DEVICES, PROCESSES, OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT THEREOF, OR OF PARTS THEREOF (EPO) E45.002 .Bistable switching devices, e.g., Ovshinsky-effect devices (EPO) E45.003Switching materials being oxides or nitrides (EPO) E45.004N: Light-controlled Ovshinsky devices (EPO) E45.005 .Charge density wave transport
current to be rectified, amplified, oscillated, or switched (EPO) E29.326Resistor with PN junction (EPO) E29.327Diode (EPO) E29.328Planar PN junction diode (EPO) E29.329Mesa PN junction diode (EPO) E29.33Hi-lo semiconductor device (e.g., memory device) (EPO) E29.331Charge trapping diode (EPO) E29.332Punchthrough diode (i.e., with bulk potential barrier	EFFECT DEVICES, PROCESSES, OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT THEREOF, OR OF PARTS THEREOF (EPO) E45.002 .Bistable switching devices, e.g., Ovshinsky-effect devices (EPO) E45.003Switching materials being oxides or nitrides (EPO) E45.004N: Light-controlled Ovshinsky devices (EPO) E45.005 .Charge density wave transport devices (EPO)
current to be rectified, amplified, oscillated, or switched (EPO) E29.326Resistor with PN junction (EPO) E29.327Diode (EPO) E29.328Planar PN junction diode (EPO) E29.329Mesa PN junction diode (EPO) E29.33Hi-lo semiconductor device (e.g., memory device) (EPO) E29.331Charge trapping diode (EPO) E29.332Punchthrough diode (i.e., with bulk potential barrier (e.g., camel diode, planar	EFFECT DEVICES, PROCESSES, OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT THEREOF, OR OF PARTS THEREOF (EPO) E45.002 .Bistable switching devices, e.g., Ovshinsky-effect devices (EPO) E45.003Switching materials being oxides or nitrides (EPO) E45.004N: Light-controlled Ovshinsky devices (EPO) E45.005 .Charge density wave transport devices (EPO) E45.006 .Solid-state travelling-wave
current to be rectified, amplified, oscillated, or switched (EPO) E29.326Resistor with PN junction (EPO) E29.327Diode (EPO) E29.328Planar PN junction diode (EPO) E29.329Mesa PN junction diode (EPO) E29.33Hi-lo semiconductor device (e.g., memory device) (EPO) E29.331Charge trapping diode (EPO) E29.332Punchthrough diode (i.e., with bulk potential barrier (e.g., camel diode, planar doped barrier diode, graded	EFFECT DEVICES, PROCESSES, OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT THEREOF, OR OF PARTS THEREOF (EPO) E45.002 .Bistable switching devices, e.g., Ovshinsky-effect devices (EPO) E45.003Switching materials being oxides or nitrides (EPO) E45.004N: Light-controlled Ovshinsky devices (EPO) E45.005 .Charge density wave transport devices (EPO) E45.006 .Solid-state travelling-wave devices (EPO)
current to be rectified, amplified, oscillated, or switched (EPO) E29.326Resistor with PN junction (EPO) E29.327Diode (EPO) E29.328Planar PN junction diode (EPO) E29.329Mesa PN junction diode (EPO) E29.33Hi-lo semiconductor device (e.g., memory device) (EPO) E29.331Charge trapping diode (EPO) E29.332Punchthrough diode (i.e., with bulk potential barrier (e.g., camel diode, planar doped barrier diode, graded bandgap diode)) (EPO)	EFFECT DEVICES, PROCESSES, OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT THEREOF, OR OF PARTS THEREOF (EPO) E45.002 .Bistable switching devices, e.g., Ovshinsky-effect devices (EPO) E45.003Switching materials being oxides or nitrides (EPO) E45.004N: Light-controlled Ovshinsky devices (EPO) E45.005 .Charge density wave transport devices (EPO) E45.006 .Solid-state travelling-wave devices (EPO) E25.001 ASSEMBLIES CONSISTING OF
current to be rectified, amplified, oscillated, or switched (EPO) E29.326Resistor with PN junction (EPO) E29.327Diode (EPO) E29.328Planar PN junction diode (EPO) E29.329Mesa PN junction diode (EPO) E29.33Hi-lo semiconductor device (e.g., memory device) (EPO) E29.331Charge trapping diode (EPO) E29.332Punchthrough diode (i.e., with bulk potential barrier (e.g., camel diode, planar doped barrier diode, graded bandgap diode)) (EPO) E29.333Point contact diode (EPO)	EFFECT DEVICES, PROCESSES, OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT THEREOF, OR OF PARTS THEREOF (EPO) E45.002 .Bistable switching devices, e.g., Ovshinsky-effect devices (EPO) E45.003Switching materials being oxides or nitrides (EPO) E45.004N: Light-controlled Ovshinsky devices (EPO) E45.005 .Charge density wave transport devices (EPO) E45.006 .Solid-state travelling-wave devices (EPO) E25.001 ASSEMBLIES CONSISTING OF PLURALITY OF INDIVIDUAL
current to be rectified, amplified, oscillated, or switched (EPO) E29.326Resistor with PN junction (EPO) E29.327Diode (EPO) E29.328Planar PN junction diode (EPO) E29.329Mesa PN junction diode (EPO) E29.33Hi-lo semiconductor device (e.g., memory device) (EPO) E29.331Charge trapping diode (EPO) E29.332Punchthrough diode (i.e., with bulk potential barrier (e.g., camel diode, planar doped barrier diode, graded bandgap diode)) (EPO) E29.333Point contact diode (EPO) E29.334Transit-time diode (e.g.,	EFFECT DEVICES, PROCESSES, OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT THEREOF, OR OF PARTS THEREOF (EPO) E45.002 .Bistable switching devices, e.g., Ovshinsky-effect devices (EPO) E45.003Switching materials being oxides or nitrides (EPO) E45.004N: Light-controlled Ovshinsky devices (EPO) E45.005 .Charge density wave transport devices (EPO) E45.006 .Solid-state travelling-wave devices (EPO) E25.001 ASSEMBLIES CONSISTING OF PLURALITY OF INDIVIDUAL SEMICONDUCTOR OR OTHER SOLID-
current to be rectified, amplified, oscillated, or switched (EPO) E29.326Resistor with PN junction (EPO) E29.327Diode (EPO) E29.328Planar PN junction diode (EPO) E29.329Mesa PN junction diode (EPO) E29.33Hi-lo semiconductor device (e.g., memory device) (EPO) E29.331Charge trapping diode (EPO) E29.332Punchthrough diode (i.e., with bulk potential barrier (e.g., camel diode, planar doped barrier diode, graded bandgap diode)) (EPO) E29.333Point contact diode (EPO) E29.334Transit-time diode (e.g., IMPATT, TRAPATT diode) (EPO)	EFFECT DEVICES, PROCESSES, OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT THEREOF, OR OF PARTS THEREOF (EPO) E45.002 .Bistable switching devices, e.g., Ovshinsky-effect devices (EPO) E45.003Switching materials being oxides or nitrides (EPO) E45.004N: Light-controlled Ovshinsky devices (EPO) E45.005 .Charge density wave transport devices (EPO) E45.006 .Solid-state travelling-wave devices (EPO) E25.001 ASSEMBLIES CONSISTING OF PLURALITY OF INDIVIDUAL SEMICONDUCTOR OR OTHER SOLID- STATE DEVICES (EPO)
current to be rectified, amplified, oscillated, or switched (EPO) E29.326Resistor with PN junction (EPO) E29.327Diode (EPO) E29.328Planar PN junction diode (EPO) E29.329Mesa PN junction diode (EPO) E29.33Hi-lo semiconductor device (e.g., memory device) (EPO) E29.331Charge trapping diode (EPO) E29.332Punchthrough diode (i.e., with bulk potential barrier (e.g., camel diode, planar doped barrier diode, graded bandgap diode)) (EPO) E29.333Point contact diode (EPO) E29.334Transit-time diode (e.g., IMPATT, TRAPATT diode) (EPO) E29.335Avalanche diode (e.g., Zener	EFFECT DEVICES, PROCESSES, OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT THEREOF, OR OF PARTS THEREOF (EPO) E45.002 .Bistable switching devices, e.g., Ovshinsky-effect devices (EPO) E45.003Switching materials being oxides or nitrides (EPO) E45.004N: Light-controlled Ovshinsky devices (EPO) E45.005 .Charge density wave transport devices (EPO) E45.006 .Solid-state travelling-wave devices (EPO) E25.001 ASSEMBLIES CONSISTING OF PLURALITY OF INDIVIDUAL SEMICONDUCTOR OR OTHER SOLID- STATE DEVICES (EPO) E25.002 .All devices being of same type,
current to be rectified, amplified, oscillated, or switched (EPO) E29.326Resistor with PN junction (EPO) E29.327Diode (EPO) E29.328Planar PN junction diode (EPO) E29.329Mesa PN junction diode (EPO) E29.33Hi-lo semiconductor device (e.g., memory device) (EPO) E29.331Charge trapping diode (EPO) E29.332Punchthrough diode (i.e., with bulk potential barrier (e.g., camel diode, planar doped barrier diode, graded bandgap diode)) (EPO) E29.333Point contact diode (EPO) E29.334Transit-time diode (e.g., IMPATT, TRAPATT diode) (EPO) E29.335Avalanche diode (e.g., Zener diode) (EPO)	EFFECT DEVICES, PROCESSES, OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT THEREOF, OR OF PARTS THEREOF (EPO) E45.002 .Bistable switching devices, e.g., Ovshinsky-effect devices (EPO) E45.003Switching materials being oxides or nitrides (EPO) E45.004N: Light-controlled Ovshinsky devices (EPO) E45.005 .Charge density wave transport devices (EPO) E45.006 .Solid-state travelling-wave devices (EPO) E25.001 ASSEMBLIES CONSISTING OF PLURALITY OF INDIVIDUAL SEMICONDUCTOR OR OTHER SOLID- STATE DEVICES (EPO)
current to be rectified, amplified, oscillated, or switched (EPO) E29.326Resistor with PN junction (EPO) E29.327Diode (EPO) E29.328Planar PN junction diode (EPO) E29.329Mesa PN junction diode (EPO) E29.33Hi-lo semiconductor device (e.g., memory device) (EPO) E29.331Charge trapping diode (EPO) E29.332Punchthrough diode (i.e., with bulk potential barrier (e.g., camel diode, planar doped barrier diode, graded bandgap diode)) (EPO) E29.333Point contact diode (EPO) E29.334Transit-time diode (e.g., IMPATT, TRAPATT diode) (EPO) E29.335Avalanche diode (e.g., Zener	EFFECT DEVICES, PROCESSES, OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT THEREOF, OR OF PARTS THEREOF (EPO) E45.002 .Bistable switching devices, e.g., Ovshinsky-effect devices (EPO) E45.003Switching materials being oxides or nitrides (EPO) E45.004N: Light-controlled Ovshinsky devices (EPO) E45.005 .Charge density wave transport devices (EPO) E45.006 .Solid-state travelling-wave devices (EPO) E25.001 ASSEMBLIES CONSISTING OF PLURALITY OF INDIVIDUAL SEMICONDUCTOR OR OTHER SOLID- STATE DEVICES (EPO) E25.002 .All devices being of same type, e.g., assemblies of rectifier
current to be rectified, amplified, oscillated, or switched (EPO) E29.326Resistor with PN junction (EPO) E29.327Diode (EPO) E29.328Planar PN junction diode (EPO) E29.329Mesa PN junction diode (EPO) E29.33Hi-lo semiconductor device (e.g., memory device) (EPO) E29.331Charge trapping diode (EPO) E29.332Punchthrough diode (i.e., with bulk potential barrier (e.g., camel diode, planar doped barrier diode, graded bandgap diode)) (EPO) E29.333Point contact diode (EPO) E29.334Transit-time diode (e.g., IMPATT, TRAPATT diode) (EPO) E29.335Avalanche diode (e.g., Zener diode) (EPO)	EFFECT DEVICES, PROCESSES, OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT THEREOF, OR OF PARTS THEREOF (EPO) E45.002 .Bistable switching devices, e.g., Ovshinsky-effect devices (EPO) E45.003Switching materials being oxides or nitrides (EPO) E45.004N: Light-controlled Ovshinsky devices (EPO) E45.005 .Charge density wave transport devices (EPO) E45.006 .Solid-state travelling-wave devices (EPO) E25.001 ASSEMBLIES CONSISTING OF PLURALITY OF INDIVIDUAL SEMICONDUCTOR OR OTHER SOLID- STATE DEVICES (EPO) E25.002 .All devices being of same type, e.g., assemblies of rectifier diodes (EPO)

E25.004	Devices responsive or sensitive to electromagnetic radiation, e.g., infrared radiation, adapted for conversion of radiation into electrical energy or for control of electrical energy by such radiation (EPO)
E25.005	Devices being arranged next to each other (EPO)
E25.006	Stacked arrangements of devices (EPO)
E25.007	Devices being solar cells (EPO)
E25.008	Organic solid-state devices (EPO)
E25.009	Devices responsive or
	sensitive to electromagnetic radiation, e.g., infrared radiation, adapted for conversion of radiation into electrical energy or for control of electrical energy by such radiation, e.g., photovoltaic modules based on organic solar cells (EPO)
E25.01	of semiconductor or other solid state devices or components formed in or on common substrate, e.g., integrated circuit device (EPO)
E25.011	Devices being arranged next and on each other, i.e., mixed assemblies (EPO)
E25.012	Devices being arranged next to each other (EPO)
E25.013	Stacked arrangements of
E25.014	devices (EPO)Semiconductor devices adapted for rectifying, amplifying, oscillating, or switching, capacitors, or resistors with at least one potential-jump barrier or surface barrier (EPO)
E25.015	Devices being arranged next and on each other, i.e., mixed
E25.016	<pre>assemblies (EPO)Devices being arranged next to each other (EPO)</pre>
E25.017	Apertured devices mounted on one or more rods passed

through apertures (EPO)

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E25.018 .... Stacked arrangements of
           nonapertured devices (EPO)
E25.019 ... Incoherent light-emitting
           semiconductor devices having
           potential or surface barrier
           (EPO)
E25.02 ....Devices being arranged next
           to each other (EPO)
E25.021 ....Stacked arrangements of
           devices (EPO)
E25.022 .. Devices having separate
           containers (EPO)
E25.023 ... Device consisting of plurality
           of semiconductor or other
           solid-state devices or
           components formed in or on
           common substrate, e.g.,
           integrated circuit device
           (EPO)
E25.024 ...Semiconductors devices adapted
           for rectifying, amplifying,
           oscillating, or switching,
           capacitors, or resistors with
           at least one potential-jump
           barrier or surface barrier
           (EPO)
E25.025 ....Mixed assemblies (EPO)
E25.026 .... Devices being arranged next
           to each other (EPO)
E25.027 ....Stacked arrangements of
           devices (EPO)
E25.028 ... Incoherent light-emitting
           semiconductor devices having
           potential or surface barrier
           (EPO)
E25.029 .Devices being of two or more
           types, e.g., forming hybrid
           circuits (EPO)
E25.03 .. Devices being mounted on two or
           more different substrates
           (EPO)
E25.031 .. Containers (EPO)
E25.032 .. Comprising optoelectronic
           devices, e.g., LED,
           photodiodes (EPO)
E23.001 PACKAGING, INTERCONNECTS, AND
           MARKINGS FOR SEMICONDUCTOR OR
           OTHER SOLID-STATE DEVICES
           (EPO)
E23.002 .Details not otherwise provided
           for, e.g., protection against
           moisture (EPO)
E23.003 .Mountings, e.g., nondetachable
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insulating substrates (EPO)

E23.004 .. Characterized by shape (EPO)

257 - 40 CLASS 257 ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID-STATE DIODES)

E23.005	Characterized by material or its electrical properties		Bases or plates or solder therefor (EPO)
E23.006	(EPO)Metallic substrates having		Having heterogeneous or anisotropic structure (EPO)
E23.007	<pre>insulating layers (EPO)Organic substrates, e.g.,</pre>		Characterized by material (EPO)
E23.008	<pre>plastic (EPO)Semiconductor insulating</pre>	E23.03	Semiconductor (EPO)Carbon (EPO)
E23.009	substrates (EPO)Ceramic or glass substrates	E23.031	Lead frames or other flat leads (EPO)
	(EPO)	E23.032	Additional leads (EPO)
E23.01	.Arrangements for conducting electric current to or from		Additional leads being bump or wire (EPO)
	solid-state body in operation, e.g., leads, terminal		Additional leads being tape carrier or flat leads (EPO)
E23 011	arrangements (EPO)Internal lead connections,	E23.035	Additional leads being
223.011	e.g., via connections,	E33 U36	<pre>multilayer (EPO)Additional leads being</pre>
	feedthrough structures (EPO)	E23.030	wiring board (EPO)
E23.012	Consisting of lead-in layers inseparably applied to	E23.037	Characterized by die pad (EPO)
maa aaa	semiconductor body (EPO)	E23.038	Insulative substrate being
E23.U13	Bridge structure with air gap (EPO)		used as die pad, e.g., ceramic, plastic (EPO)
E23.014	Beam leads (EPO)	E23.039	Chip-on-leads or leads-on-
E23.015	Pads with extended contours, e.g., grid structure, branch structure, finger structure	220,000	chip techniques, i.e., inner lead fingers being used as die pad (EPO)
T02 016	(EPO)	E23.04	Having bonding material
E23.016	For devices consisting of		between chip and die pad (EPO)
	semiconductor layers on insulating or semi-insulating		Multilayer (EPO)
	substrates, e.g., silicon on	E23.042	Plurality of lead frames
	sapphire devices, i.e., SOS	₽22 042	mounted in one device (EPO)Geometry of lead frame (EPO)
	(EPO)		For devices adapted for
	Materials (EPO)	H25.011	rectifying, amplifying,
E23.018	Conductive organic material		oscillating, or switching,
	or pastes, e.g., conductive adhesives, inks (EPO)		capacitors, or resistors with at least one potential-jump
E23.019	Consisting of layered		barrier or surface barrier
	constructions comprising		(EPO)
	conductive layers and	E23.045	Deformation absorbing parts
	insulating layers, e.g., planar contacts (EPO)		in lead frame plane, e.g.,
E23.02	Bonding areas, e.g., pads		meanderline shape (EPO)
	(EPO)		Cross-section geometry (EPO)Characterized by bent parts
	Bump or ball contacts (EPO)		(EPO)
	Overhang structure (EPO)	E23.048	Bent parts being outer
E23.023	Consisting of soldered or		leads (EPO)
E33 U34	bonded constructions (EPO)Wire-like arrangements or pins	E23.049	Insulating layers on lead
127.02T	or rods (EPO)		frame, e.g., bridging members
E23.025	Characterized by materials of	E23.05	(EPO)
	wires or their coatings (EPO)	EZ3.U3	<pre>Side rails of lead frame, e.g., with perforations, sprocket holes (EPO)</pre>

e.g., use of heat pipes (EPO)

E23.051Specifically adapted to facilitate heat dissipation	E23.071For devices adapted for rectifying, amplifying,
(EPO) E23.052Assembly of semiconductor devices on lead frame (EPO)	oscillating, or switching, capacitors, or resistors with at least one potential-jump
E23.053Characterized by materials of lead frames or layers thereon (EPO)	barrier or surface barrier (EPO) E23.072Characterized by materials
E23.054Metallic layers on lead frames (EPO)	(EPO) E23.073Conductive materials
E23.055Consisting of thin flexible metallic tape with or without	containing semiconductor material (EPO)
film carrier (EPO) E23.056Insulating layers on lead	E23.074Carbon, e.g., fullerenes (EPO)
frames (EPO) E23.057Capacitor integral with or on	E23.075Conductive materials containing organic materials
lead frame (EPO) E23.058Battery in combination with	or pastes, e.g., for thick films (EPO)
lead frame (EPO) E23.059Oscillators in combination	E23.076Conductive materials containing superconducting
with lead frame (EPO) E23.06Leads, i.e., metallizations or	<pre>material (EPO) E23.077Materials of insulating</pre>
lead frames on insulating substrates, e.g., chip carriers (EPO)	layers or coatings (EPO) E23.078Flexible arrangements, e.g., pressure contacts without
E23.061Leads being also applied on sidewalls or bottom of substrate, e.g., leadless	soldering (EPO) E23.079For integrated circuit devices, e.g., power bus, number of
<pre>packages for surface mounting (EPO)</pre>	leads (EPO) E23.08 .Arrangements for cooling,
E23.062Multilayer substrates (EPO) E23.063Chip support structure consisting of plurality of	heating, ventilating or temperature compensation; temperature-sensing arrangements (EPO)
insulating substrates (EPO) E23.064For flat cards, e.g., credit	E23.081Arrangements for heating (EPO) E23.082Cooling arrangements using
cards (EPO) E23.065Flexible insulating	Peltier effect (EPO) E23.083Mountings or securing means for
substrates (EPO) E23.066Lead frames fixed on or encapsulated in insulating substrates (EPO)	detachable cooling or heating arrangements; fixed by friction, plugs or springs
E23.067Via connections through substrates, e.g., pins going	(EPO) E23.084With bolts or screws (EPO) E23.085For stacked arrangements of
through substrate, coaxial cables (EPO)	plurality of semiconductor devices (EPO)
E23.068Additional leads joined to metallizations on insulating substrate, e.g., pins, bumps,	E23.086Snap-on arrangements, e.g., clips (EPO)
wires, flat leads (EPO) E23.069Spherical bumps on substrate	E23.087Fillings or auxiliary members in containers or encapsulations selected or
for external connection, e.g., ball grid arrays (BGA) (EPO) F23 07 Cormetry or layout (EPO)	arranged to facilitate heating or cooling (EPO)
E23.07Geometry or layout (EPO)	E23.088Cooling by change of state,

257 - 42 CLASS 257 ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID-STATE DIODES)

E23.089	By melting or evaporation of solids (EPO)	E23.112	Having heterogeneous or anisotropic structure, e.g.,
E23.09	Auxiliary members in		powder or fibers in matrix,
	containers characterized by		wire mesh, porous structures
	their shape, e.g., pistons		(EPO)
	(EPO)	F23 113	Ceramic materials or glass
поэ оо1		E25.115	
	Bellows (EPO)	-00 114	(EPO)
E23.092	Auxiliary members in	E23.114	.Protection against radiation,
	encapsulations (EPO)		e.g., light, electromagnetic
E23.093	In combination with jet		waves (EPO)
	impingement (EPO)		Against alpha rays (EPO)
E23.094	Pistons, e.g., spring-loaded	E23.116	.Encapsulations, e.g.,
	members (EPO)		encapsulating layers,
E23.095	Complete device being wholly		coatings, e.g., for protection
	immersed in fluid other than		(EPO)
	air (EPO)	E23.117	Characterized by material,
E23 096	Fluid being liquefied gas,		e.g., carbon (EPO)
L23.0 70	e.g., in cryogenic vessel	E23.118	Oxides or nitrides or
	(EPO)		carbides, e.g., ceramics,
E22 007			glass (EPO)
E23.097	Involving transfer of heat by	F23 110	Organic, e.g., plastic, epoxy
T02 000	flowing fluids (EPO)	E23.117	(EPO)
	By flowing liquids (EPO)	maa 1a	
E23.099	By flowing gases, e.g., air	E23.12	Organo-silicon compounds,
	(EPO)	T02 101	e.g., silicone (EPO)
	Jet impingement (EPO)		Containing filler (EPO)
E23.101	Selection of materials, or	E23.122	Semiconductor material, e.g.,
	shaping, to facilitate cooling		amorphous silicon (EPO)
	or heating, e.g., heat sinks	E23.123	Characterized by arrangement or
	or heating, e.g., heat sinks (EPO)	E23.123	Characterized by arrangement or shape (EPO)
E23.102			
E23.102	(EPO)		shape (EPO)
	<pre>(EPO)Cooling facilitated by shape of device (EPO)</pre>	E23.124	<pre>shape (EPO)Device being completely</pre>
	(EPO)Cooling facilitated by shape	E23.124	<pre>shape (EPO)Device being completely enclosed (EPO)</pre>
E23.103	<pre>(EPO)Cooling facilitated by shape of device (EPO)Foil-like cooling fins or heat sinks (EPO)</pre>	E23.124 E23.125	<pre>shape (EPO)Device being completely enclosed (EPO)Substrate forming part of encapsulation (EPO)</pre>
E23.103	<pre>(EPO)Cooling facilitated by shape of device (EPO)Foil-like cooling fins or heat sinks (EPO)Characterized by shape of</pre>	E23.124 E23.125	<pre>shape (EPO)Device being completely enclosed (EPO)Substrate forming part of encapsulation (EPO)Double encapsulation or</pre>
E23.103	<pre>(EPO)Cooling facilitated by shape of device (EPO)Foil-like cooling fins or heat sinks (EPO)Characterized by shape of housing (EPO)</pre>	E23.124 E23.125	<pre>shape (EPO)Device being completely enclosed (EPO)Substrate forming part of encapsulation (EPO)Double encapsulation or coating and encapsulation</pre>
E23.103	<pre>(EPO)Cooling facilitated by shape of device (EPO)Foil-like cooling fins or heat sinks (EPO)Characterized by shape of housing (EPO)Wire-like or pin-like cooling</pre>	E23.124 E23.125 E23.126	<pre>shape (EPO)Device being completely enclosed (EPO)Substrate forming part of encapsulation (EPO)Double encapsulation or coating and encapsulation (EPO)</pre>
E23.103 E23.104 E23.105	<pre>(EPO)Cooling facilitated by shape of device (EPO)Foil-like cooling fins or heat sinks (EPO)Characterized by shape of housing (EPO)Wire-like or pin-like cooling fins or heat sinks (EPO)</pre>	E23.124 E23.125 E23.126	<pre>shape (EPO)Device being completely enclosed (EPO)Substrate forming part of encapsulation (EPO)Double encapsulation or coating and encapsulation (EPO)Sealing arrangements between</pre>
E23.103 E23.104 E23.105 E23.106	<pre>(EPO)Cooling facilitated by shape of device (EPO)Foil-like cooling fins or heat sinks (EPO)Characterized by shape of housing (EPO)Wire-like or pin-like cooling fins or heat sinks (EPO)Laminates or multilayers,</pre>	E23.124 E23.125 E23.126	<pre>shape (EPO)Device being completely enclosed (EPO)Substrate forming part of encapsulation (EPO)Double encapsulation or coating and encapsulation (EPO)Sealing arrangements between parts, e.g., adhesion</pre>
E23.103 E23.104 E23.105 E23.106	<pre>(EPO)Cooling facilitated by shape of device (EPO)Foil-like cooling fins or heat sinks (EPO)Characterized by shape of housing (EPO)Wire-like or pin-like cooling fins or heat sinks (EPO)Laminates or multilayers, e.g., direct bond copper</pre>	E23.124 E23.125 E23.126 E23.127	<pre>shape (EPO)Device being completely enclosed (EPO)Substrate forming part of encapsulation (EPO)Double encapsulation or coating and encapsulation (EPO)Sealing arrangements between parts, e.g., adhesion promoters (EPO)</pre>
E23.103 E23.104 E23.105 E23.106	<pre>(EPO)Cooling facilitated by shape of device (EPO)Foil-like cooling fins or heat sinks (EPO)Characterized by shape of housing (EPO)Wire-like or pin-like cooling fins or heat sinks (EPO)Laminates or multilayers, e.g., direct bond copper ceramic substrates (EPO)</pre>	E23.124 E23.125 E23.126 E23.127	shape (EPO)Device being completely enclosed (EPO)Substrate forming part of encapsulation (EPO)Double encapsulation or coating and encapsulation (EPO)Sealing arrangements between parts, e.g., adhesion promoters (EPO)Encapsulation having cavity
E23.103 E23.104 E23.105 E23.106	<pre>(EPO)Cooling facilitated by shape of device (EPO)Foil-like cooling fins or heat sinks (EPO)Characterized by shape of housing (EPO)Wire-like or pin-like cooling fins or heat sinks (EPO)Laminates or multilayers, e.g., direct bond copper ceramic substrates (EPO)Organic materials with or</pre>	E23.124 E23.125 E23.126 E23.127 E23.128	shape (EPO)Device being completely enclosed (EPO)Substrate forming part of encapsulation (EPO)Double encapsulation or coating and encapsulation (EPO)Sealing arrangements between parts, e.g., adhesion promoters (EPO)Encapsulation having cavity (EPO)
E23.103 E23.104 E23.105 E23.106	<pre>(EPO)Cooling facilitated by shape of device (EPO)Foil-like cooling fins or heat sinks (EPO)Characterized by shape of housing (EPO)Wire-like or pin-like cooling fins or heat sinks (EPO)Laminates or multilayers, e.g., direct bond copper ceramic substrates (EPO)Organic materials with or without thermo-conductive</pre>	E23.124 E23.125 E23.126 E23.127 E23.128	shape (EPO)Device being completely enclosed (EPO)Substrate forming part of encapsulation (EPO)Double encapsulation or coating and encapsulation (EPO)Sealing arrangements between parts, e.g., adhesion promoters (EPO)Encapsulation having cavity (EPO)Partial encapsulation or
E23.103 E23.104 E23.105 E23.106 E23.107	<pre>(EPO)Cooling facilitated by shape of device (EPO)Foil-like cooling fins or heat sinks (EPO)Characterized by shape of housing (EPO)Wire-like or pin-like cooling fins or heat sinks (EPO)Laminates or multilayers, e.g., direct bond copper ceramic substrates (EPO)Organic materials with or without thermo-conductive filler (EPO)</pre>	E23.124 E23.125 E23.126 E23.127 E23.128 E23.129	shape (EPO)Device being completely enclosed (EPO)Substrate forming part of encapsulation (EPO)Double encapsulation or coating and encapsulation (EPO)Sealing arrangements between parts, e.g., adhesion promoters (EPO)Encapsulation having cavity (EPO)Partial encapsulation or coating (EPO)
E23.103 E23.104 E23.105 E23.106 E23.107	<pre>(EPO)Cooling facilitated by shape of device (EPO)Foil-like cooling fins or heat sinks (EPO)Characterized by shape of housing (EPO)Wire-like or pin-like cooling fins or heat sinks (EPO)Laminates or multilayers, e.g., direct bond copper ceramic substrates (EPO)Organic materials with or without thermo-conductive filler (EPO)Semiconductor materials (EPO)</pre>	E23.124 E23.125 E23.126 E23.127 E23.128 E23.129 E23.13	shape (EPO)Device being completely enclosed (EPO)Substrate forming part of encapsulation (EPO)Double encapsulation or coating and encapsulation (EPO)Sealing arrangements between parts, e.g., adhesion promoters (EPO)Encapsulation having cavity (EPO)Partial encapsulation or coating (EPO)Coating being foil (EPO)
E23.103 E23.104 E23.105 E23.106 E23.107	<pre>(EPO)Cooling facilitated by shape of device (EPO)Foil-like cooling fins or heat sinks (EPO)Characterized by shape of housing (EPO)Wire-like or pin-like cooling fins or heat sinks (EPO)Laminates or multilayers, e.g., direct bond copper ceramic substrates (EPO)Organic materials with or without thermo-conductive filler (EPO)</pre>	E23.124 E23.125 E23.126 E23.127 E23.128 E23.129 E23.13	shape (EPO)Device being completely enclosed (EPO)Substrate forming part of encapsulation (EPO)Double encapsulation or coating and encapsulation (EPO)Sealing arrangements between parts, e.g., adhesion promoters (EPO)Encapsulation having cavity (EPO)Partial encapsulation or coating (EPO)Coating being foil (EPO)Coating or filling in grooves
E23.103 E23.104 E23.105 E23.106 E23.107	<pre>(EPO)Cooling facilitated by shape of device (EPO)Foil-like cooling fins or heat sinks (EPO)Characterized by shape of housing (EPO)Wire-like or pin-like cooling fins or heat sinks (EPO)Laminates or multilayers, e.g., direct bond copper ceramic substrates (EPO)Organic materials with or without thermo-conductive filler (EPO)Semiconductor materials (EPO)</pre>	E23.124 E23.125 E23.126 E23.127 E23.128 E23.129 E23.13	shape (EPO)Device being completely enclosed (EPO)Substrate forming part of encapsulation (EPO)Double encapsulation or coating and encapsulation (EPO)Sealing arrangements between parts, e.g., adhesion promoters (EPO)Encapsulation having cavity (EPO)Partial encapsulation or coating (EPO)Coating being foil (EPO)Coating or filling in grooves made in semiconductor body
E23.103 E23.104 E23.105 E23.106 E23.107 E23.108 E23.109	<pre>(EPO)Cooling facilitated by shape of device (EPO)Foil-like cooling fins or heat sinks (EPO)Characterized by shape of housing (EPO)Wire-like or pin-like cooling fins or heat sinks (EPO)Laminates or multilayers, e.g., direct bond copper ceramic substrates (EPO)Organic materials with or without thermo-conductive filler (EPO)Semiconductor materials (EPO)Metallic materials (EPO)</pre>	E23.124 E23.125 E23.126 E23.127 E23.128 E23.129 E23.13 E23.131	shape (EPO)Device being completely enclosed (EPO)Substrate forming part of encapsulation (EPO)Double encapsulation or coating and encapsulation (EPO)Sealing arrangements between parts, e.g., adhesion promoters (EPO)Encapsulation having cavity (EPO)Partial encapsulation or coating (EPO)Coating being foil (EPO)Coating or filling in grooves made in semiconductor body (EPO)
E23.103 E23.104 E23.105 E23.106 E23.107 E23.108 E23.109	<pre>(EPO)Cooling facilitated by shape of device (EPO)Foil-like cooling fins or heat sinks (EPO)Characterized by shape of housing (EPO)Wire-like or pin-like cooling fins or heat sinks (EPO)Laminates or multilayers, e.g., direct bond copper ceramic substrates (EPO)Organic materials with or without thermo-conductive filler (EPO)Semiconductor materials (EPO)Metallic materials (EPO)Cooling facilitated by</pre>	E23.124 E23.125 E23.126 E23.127 E23.128 E23.129 E23.13 E23.131	shape (EPO)Device being completely enclosed (EPO)Substrate forming part of encapsulation (EPO)Double encapsulation or coating and encapsulation (EPO)Sealing arrangements between parts, e.g., adhesion promoters (EPO)Encapsulation having cavity (EPO)Partial encapsulation or coating (EPO)Coating being foil (EPO)Coating or filling in grooves made in semiconductor body
E23.103 E23.104 E23.105 E23.106 E23.107 E23.108 E23.109	<pre>(EPO)Cooling facilitated by shape of device (EPO)Foil-like cooling fins or heat sinks (EPO)Characterized by shape of housing (EPO)Wire-like or pin-like cooling fins or heat sinks (EPO)Laminates or multilayers, e.g., direct bond copper ceramic substrates (EPO)Organic materials with or without thermo-conductive filler (EPO)Semiconductor materials (EPO)Metallic materials (EPO)Cooling facilitated by selection of materials for</pre>	E23.124 E23.125 E23.126 E23.127 E23.128 E23.129 E23.13 E23.131	shape (EPO)Device being completely enclosed (EPO)Substrate forming part of encapsulation (EPO)Double encapsulation or coating and encapsulation (EPO)Sealing arrangements between parts, e.g., adhesion promoters (EPO)Encapsulation having cavity (EPO)Partial encapsulation or coating (EPO)Coating being foil (EPO)Coating or filling in grooves made in semiconductor body (EPO)
E23.103 E23.104 E23.105 E23.106 E23.107 E23.108 E23.109	<pre>(EPO)Cooling facilitated by shape of device (EPO)Foil-like cooling fins or heat sinks (EPO)Characterized by shape of housing (EPO)Wire-like or pin-like cooling fins or heat sinks (EPO)Laminates or multilayers, e.g., direct bond copper ceramic substrates (EPO)Organic materials with or without thermo-conductive filler (EPO)Semiconductor materials (EPO)Metallic materials (EPO)Cooling facilitated by selection of materials for device (or materials for</pre>	E23.124 E23.125 E23.126 E23.127 E23.128 E23.129 E23.13 E23.131	shape (EPO)Device being completely enclosed (EPO)Substrate forming part of encapsulation (EPO)Double encapsulation or coating and encapsulation (EPO)Sealing arrangements between parts, e.g., adhesion promoters (EPO)Encapsulation having cavity (EPO)Partial encapsulation or coating (EPO)Coating being foil (EPO)Coating or filling in grooves made in semiconductor body (EPO)Coating being directly
E23.103 E23.104 E23.105 E23.106 E23.107 E23.108 E23.109 E23.11	<pre>(EPO)Cooling facilitated by shape of device (EPO)Foil-like cooling fins or heat sinks (EPO)Characterized by shape of housing (EPO)Wire-like or pin-like cooling fins or heat sinks (EPO)Laminates or multilayers, e.g., direct bond copper ceramic substrates (EPO)Organic materials with or without thermo-conductive filler (EPO)Semiconductor materials (EPO)Metallic materials (EPO)Metallic materials for device (or materials for thermal expansion adaptation,</pre>	E23.124 E23.125 E23.126 E23.127 E23.128 E23.129 E23.13 E23.131	shape (EPO)Device being completely enclosed (EPO)Substrate forming part of encapsulation (EPO)Double encapsulation or coating and encapsulation (EPO)Sealing arrangements between parts, e.g., adhesion promoters (EPO)Encapsulation having cavity (EPO)Partial encapsulation or coating (EPO)Coating being foil (EPO)Coating or filling in grooves made in semiconductor body (EPO)Coating being directly applied to semiconductor body, e.g., passivation layer (EPO)Coating also covering
E23.103 E23.104 E23.105 E23.106 E23.107 E23.108 E23.109 E23.11	<pre>(EPO)Cooling facilitated by shape of device (EPO)Foil-like cooling fins or heat sinks (EPO)Characterized by shape of housing (EPO)Wire-like or pin-like cooling fins or heat sinks (EPO)Laminates or multilayers, e.g., direct bond copper ceramic substrates (EPO)Organic materials with or without thermo-conductive filler (EPO)Semiconductor materials (EPO)Metallic materials (EPO)Metallic materials for device (or materials for thermal expansion adaptation, e.g., carbon) (EPO)</pre>	E23.124 E23.125 E23.126 E23.127 E23.128 E23.129 E23.13 E23.131	shape (EPO)Device being completely enclosed (EPO)Substrate forming part of encapsulation (EPO)Double encapsulation or coating and encapsulation (EPO)Sealing arrangements between parts, e.g., adhesion promoters (EPO)Encapsulation having cavity (EPO)Partial encapsulation or coating (EPO)Coating being foil (EPO)Coating or filling in grooves made in semiconductor body (EPO)Coating being directly applied to semiconductor body, e.g., passivation layer (EPO)
E23.103 E23.104 E23.105 E23.106 E23.107 E23.108 E23.109 E23.11	<pre>(EPO)Cooling facilitated by shape of device (EPO)Foil-like cooling fins or heat sinks (EPO)Characterized by shape of housing (EPO)Wire-like or pin-like cooling fins or heat sinks (EPO)Laminates or multilayers, e.g., direct bond copper ceramic substrates (EPO)Organic materials with or without thermo-conductive filler (EPO)Semiconductor materials (EPO)Metallic materials (EPO)Metallic materials for device (or materials for thermal expansion adaptation, e.g., carbon) (EPO)</pre>	E23.124 E23.125 E23.126 E23.127 E23.128 E23.129 E23.13 E23.131	shape (EPO)Device being completely enclosed (EPO)Substrate forming part of encapsulation (EPO)Double encapsulation or coating and encapsulation (EPO)Sealing arrangements between parts, e.g., adhesion promoters (EPO)Encapsulation having cavity (EPO)Partial encapsulation or coating (EPO)Coating being foil (EPO)Coating or filling in grooves made in semiconductor body (EPO)Coating being directly applied to semiconductor body, e.g., passivation layer (EPO)Coating also covering
E23.103 E23.104 E23.105 E23.106 E23.107 E23.108 E23.109 E23.11	<pre>(EPO)Cooling facilitated by shape of device (EPO)Foil-like cooling fins or heat sinks (EPO)Characterized by shape of housing (EPO)Wire-like or pin-like cooling fins or heat sinks (EPO)Laminates or multilayers, e.g., direct bond copper ceramic substrates (EPO)Organic materials with or without thermo-conductive filler (EPO)Semiconductor materials (EPO)Metallic materials (EPO)Metallic materials for device (or materials for thermal expansion adaptation, e.g., carbon) (EPO)</pre>	E23.124 E23.125 E23.126 E23.127 E23.128 E23.129 E23.13 E23.131	shape (EPO)Device being completely enclosed (EPO)Substrate forming part of encapsulation (EPO)Double encapsulation or coating and encapsulation (EPO)Sealing arrangements between parts, e.g., adhesion promoters (EPO)Encapsulation having cavity (EPO)Partial encapsulation or coating (EPO)Coating being foil (EPO)Coating or filling in grooves made in semiconductor body (EPO)Coating being directly applied to semiconductor body, e.g., passivation layer (EPO)Coating also covering sidewalls of semiconductor

E23.135	.Fillings or auxiliary members in	E23.15
	containers or encapsulations,	
	e.g., centering rings (EPO)	
E23.136	Fillings characterized by	
	material, its physical or	E23.151
	chemical properties, or its	
	arrangement within complete	
E02 12E	device (EPO)	E23.152
E23.137	Including materials for	-02 152
	absorbing or reacting with moisture or other undesired	E23.153
	substances, e.g., getters	E23.154
	(EPO)	E23.154
E23.138	Gaseous at normal operating	E23.155
	temperature of device (EPO)	E23.156
E23.139	Liquid at normal operating	123.130
	temperature of device (EPO)	E23.157
E23.14	Solid or gel at normal	
	operating temperature of	E23.158
	device (EPO)	i
E23.141	.Arrangements for conducting	E23.159
	electric current within device	E23.16
	in operation from one	,
	component to another,	,
	<pre>interconnections, e.g., wires, lead frames (EPO)</pre>]
E23 142	Including external	E23.161
123.112	interconnections consisting of	T02 160
	multilayer structure of	E23.162
	conductive and insulating	E23.163
	layers inseparably formed on	E23.103
	semiconductor body (EPO)	E23.164
E23.143	Crossover interconnections	123.101
	(EPO)	
E23.144	Capacitive arrangements or	E23.165
	effects of, or between wiring	:
E00 14E	layers (EPO)Via connections in multilevel	E23.166
E23.145	interconnection structure	
	(EPO)	
E23 146	With adaptable	:
223.110	interconnections (EPO)	E23.167
E23.147	Comprising antifuses, i.e.,	E23.168I
	connections having their state	
	changed from nonconductive to	E23.169I
	conductive (EPO)	E43.1091
E23.148	Change of state resulting	
	from use of external beam,	
	e.g., laser beam or ion beam	·
E02 140	(EPO)	E23.17

E23.149Comprising fuses, i.e.,

nonconductive (EPO)

connections having their state changed from conductive to

E23.15	<pre>Change of state resulting from use of external beam, e.g., laser beam or ion beam (EPO)</pre>
E23.151	Geometry or layout of interconnection structure (EPO)
E23.152	Cross-sectional geometry (EPO)
E23.153	Arrangements of power or ground buses (EPO)
E23.154	Characterized by materials (EPO)
E23.155	Conductive materials (EPO)
	Containing superconducting materials (EPO)
E23.157	Based on metals, e.g., alloys, metal silicides (EPO)
E23.158	Principal metal being aluminum (EPO)
E23.159	Aluminum alloys (EPO)
E23.16	Additional layers
	associated with aluminum layers, e.g., adhesion, barrier, cladding layers (EPO)
E23.161	Principal metal being copper (EPO)
E23.162	<pre>Principal metal being noble metal, e.g., gold (EPO)</pre>
E23.163	Principal metal being refractory metal (EPO)
E23.164	<pre>Containing semiconductor material, e.g., polysilicon (EPO)</pre>
E23.165	Containing carbon, e.g., fullerenes (EPO)
E23.166	Containing conductive organic materials or pastes, e.g., conductive adhesives, inks (EPO)
E23.167	Insulating materials (EPO)
E23.168	Including internal interconnections, e.g., cross-under constructions (EPO)
E23.169	Interconnection structure between plurality of semiconductor chips being formed on or in insulating substrates (EPO)
E23.17	<pre>Crossover interconnections, e.g., bridge stepovers (EPO)</pre>
E23.171	Adaptable interconnections, e.g., for engineering changes (EPO)

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E23.172	Assembly of plurality of insulating substrates (EPO)	E23.191	Char
E23.173	Multilayer substrates (EPO)		pro
	Conductive vias through substrate with or without	E23.192	Mat
	pins, e.g., buried coaxial	E23.193	Char
	conductors (EPO)		arr
E23.175	Geometry or layout of		par
	interconnection structure		bas
	(EPO)		lea
E23.176	For flat cards, e.g., credit		(EP
	cards (EPO)	E23.194	
E23 177	Flexible insulating substrates		dam
223.17,	(EPO)	E49.001	SOLID-
F23 178	Chips being integrally		ONE
E23.170	enclosed by interconnect and		SUR
	support structures (EPO)		LAY
E23 179	.Marks applied to semiconductor		CON
123.17	devices or parts, e.g.,		ADJ.
	registration marks, test		WHI
	patterns, alignment		OCC
	structures, wafer maps (EPO)		PEC
E23.18	.Containers; seals (EPO)		TRE
	Characterized by shape of		OF
	container or parts, e.g.,	E49.002	.Devic
	caps, walls (EPO)		ins
E23.182	Container being hollow		fie
	construction having no base	E49.003	.Quant
	used as mounting for		int
	semiconductor body (EPO)		sin
E23.183	Container being hollow		(EP
	construction and having	E49.004	.Thin-
	conductive base as mounting as		(EP
	well as lead for the	E21.001	PROCES
	semiconductor body (EPO)		FOR
E23.184	Other leads having insulating		OF
	passage through base (EPO)		STA
E23.185	Other leads being parallel to	=01 000	THE
	base (EPO)	E21.002	
E23.186	Other leads being	T01 002	sem
	perpendicular to base (EPO)	E21.003	
E23.187	Another lead being formed by		com
	cover plate parallel to base	T01 004	cir
	plate, e.g., sandwich type	E21.004	
	(EPO)	E21.005	
E23.188	Container being hollow		car
	construction and having	-01 006	dia
	insulating or insulated base	E21.006	
	as mounting for semiconductor		ref
	body (EPO)		nob
E23.189	Leads being parallel to base		e.g
	(EPO)	E01 007	nit
E23.19	Leads having passage through	E21.007	ora
	l (EDO)		O.r.a

- E23.191 ..Characterized by material of container or its electrical properties (EPO)
- E23.192 ...Material being electrical insulator, e.g., glass (EPO)
- E23.193 ..Characterized by material or arrangement of seals between parts, e.g., between cap and base of container or between leads and walls of container (EPO)
- E23.194 .Protection against mechanical damage (EPO)
- E49.001 SOLID-STATE DEVICES WITH AT LEAST
 ONE POTENTIAL-JUMP BARRIER OR
 SURFACE BARRIER USING ACTIVE
 LAYER OF LOWER ELECTRICAL
 CONDUCTIVITY THAN MATERIAL
 ADJACENT THERETO AND THROUGH
 WHICH CARRIER TUNNELING
 OCCURS, PROCESSES OR APPARATUS
 PECULIAR TO MANUFACTURE OR
 TREATMENT OF SUCH DEVICES, OR
 OF PARTS THEREOF (EPO)
- E49.002 .Devices using Mott metalinsulator transition, e.g., field-effect transistors (EPO)
- E49.003 .Quantum devices, e.g., quantum interference devices, metal single electron transistor (EPO)
- E49.004 .Thin-film or thick-film devices (EPO)
- E21.001 PROCESSES OR APPARATUS ADAPTED

 FOR MANUFACTURE OR TREATMENT

 OF SEMICONDUCTOR OR SOLID
 STATE DEVICES OR OF PARTS

 THEREOF (EPO)
- E21.002 .Manufacture or treatment of semiconductor device (EPO)
- E21.003 ..Manufacture of two-terminal component for integrated circuit (EPO)
- E21.004 ...Of resistor (EPO)
- E21.005Active material comprising carbon, e.g., diamond or diamond-like carbon (EPO)
- E21.006Active material comprising refractory, transition, or noble metal or metal compound, e.g., alloy, silicide, oxide, nitride (EPO)
- E21.007Active material comprising organic conducting material, e.g., conducting polymer (EPO)
- E21.008 ...Of capacitor (EPO)

base (EPO)

E21.009	Dielectric having perovskite structure (EPO)	E21.033	Comprising inorganic layer (EPO)
E21.01	<pre>Dielectric comprising two or more layers, e.g., buffer layers, seed layers, gradient layers (EPO)</pre>		<pre>For lift-off process (EPO)Characterized by their composition, e.g., multilayer masks, materials (EPO)</pre>
	Formation of electrode (EPO)With increased surface area, e.g., by roughening, texturing (EPO)	E21.036	<pre>Characterized by their size, orientation, disposition, behavior, shape, in horizontal or vertical plane (EPO)</pre>
	With rough surface, e.g., using hemispherical grains (EPO)	E21.037	Characterized by their behavior during process, e.g., soluble mask, re-deposited
	<pre>Having cylindrical, crown, or fin-type shape (EPO)Having horizontal</pre>	E21.038	<pre>mask (EPO)Characterized by process involved to create mask, e.g.,</pre>
	<pre>extensions (EPO)Made by depositing layers,</pre>		<pre>lift-off mask, sidewalls, or to modify mask, such as pre- treatment, post-treatment</pre>
E21.017	<pre>e.g., alternatingly conductive and insulating layers (EPO)Made by patterning layers,</pre>	E21.039	(EPO)Process specially adapted to
	<pre>e.g., etching conductive layers (EPO)</pre>	T01 04	improve the resolution of the mask (EPO)
E21.018	Having vertical extensions (EPO)	E21.U4	Device having at least one potential-jump barrier or
E21.019	<pre>Made by depositing layers, e.g., alternatingly conductive and insulating layers (EPO)</pre>		surface barrier, e.g., PN junction, depletion layer, carrier concentration layer
E21.02	<pre>Made by patterning layers, e.g., etching conductive layers (EPO)</pre>	E21.041	(EPO)Device having semiconductor body comprising carbon, e.g.,
E21.021	Having multilayers, e.g., comprising barrier layer and	F21 042	<pre>diamond, diamond-like carbon (EPO)Making n- or p-doped regions</pre>
E21.022	metal layer (EPO)Of inductor (EPO)		(EPO)
E21.023	Making mask on semicond uctor body for further	E21.043	Using ion im plantation (EPO)
	photolithographic processing (EPO)		Changing their shape, e.g., forming recess (EPO)
	Comprising organic layer (EPO)		Making electrode (EPO)
	For lift-off process (EPO)		Ohmic electrode (EPO)
	<pre>Characterized by treatment of photoresist layer (EPO)</pre>		Schottky electrode (EPO)Conductor-insulator-
E21.027	<pre>Photolith ographic process (EPO)</pre>		semiconductor electrode, e.g., MIS contacts (EPO)
E21.028	Using laser (EPO)	E21.049	Multistep processes for
E21.029	Using anti-reflective coating (EPO)		manufacture of device whose active layer, e.g., base,
E21.03	Electro-lithographic process (EPO)		channel, comprises semiconducting carbon, e.g.,
E21.031	X-ray lithographic process (EPO)		<pre>diamond, diamond-like carbon (EPO)</pre>
E21.032	Ion lithographic process (EPO)		

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E21.05	Device controllable only by electric current supplied or the electric potential applied to electrode which does not carry current to be rectified, amplified, or switched, e.g., three-terminal devices such as source, drain, and gate terminals; emitter, base, collector terminals (EPO)		Device controllable only by variation of electric current supplied or electric potential applied to one or more of the electrodes carrying current to be rectified, amplified, oscillated, or switched, e.g., two-terminal device (EPO)Device having semiconductor body comprising selenium (Se)
E21.051	Field-effect transistor (EPO)	E21 069	or tellurium (Te) (EPO)Preparation of substrate or
E21.052	Device controllable only by variation of electric current	121.009	foundation plate for Se or Te semiconductor (EPO)
	supplied or the electric potential applied to electrodes carrying current to be rectified, amplified,	E21.07	or Te, its application to substrate, or the subsequent treatment of combination (EPO)
₽21 0 E2	oscillated, or switched, e.g., two-terminal device (EPO) Diode (EPO)	E21.071	Application of Se or Te to substrate or foundation plate
	Device having semiconductor	E01 070	(EPO)Conversion of Se or Te to
E21.034	body comprising silicon carbide (SiC) (EPO)		conductive state (EPO)
E21.055	Passivating silicon carbide surface (EPO)	E21.0/3	Treatment of surface of Se or Te layer after having been made conductive (EPO)
E21.056	Making n- or p- doped regions	E21 074	Provision of discrete
	or layers, e.g., using diffusion (EPO)Using ion implantation (EPO)		insulating layer, i.e., specified barrier layer material (EPO)
	Using masks (EPO)	E21.075	Application of electrode to
	Angled implantation (EPO)		exposed surface of Se or Te
E21.06	<pre>Changing shape of semiconductor body, e.g., forming recesses (EPO)</pre>		after Se or Te has been applied to foundation plate (EPO)
E21.061	Making electrode (EPO)	E21.076	Treatment of complete device,
E21.062	Ohmic electrode (EPO)Conductor-insulator-		e.g., by electroforming to form barrier (EPO)
111.005	semiconductor electrode, e.g.,	E21.077	Heat treating (EPO)
	MIS contact (EPO)	E21.078	Device having semiconductor
	Schottky electrode (EPO)		body comprising cuprous oxide
E21.065	Multistep processes for		(Cu 2 0) or cuprous iodide (CuI) (EPO)
	<pre>manufacture of device whose active layer, e.g., base,</pre>	E21.079	Preparation of substrate,
	channel, comprises silicon		preliminary treatment
	carbide (EPO)		oxidation of substrate,
E21.066	\ldots Device controllable only by		reduction treatment (EPO)
	electric current supplied or	E21.08	Preliminary treatment of foundation plate (EPO)
	the electric potential applied to electrode which does not	E21.081	Reduction of copper oxide,
	carry current to be rectified,		treatment of oxide layer (EPO)
	amplified, or switched, e.g.,	E21.082	Oxidation and subsequent
	three-terminal device (EPO)		heat treatment of substrate (EPO)
		E21.083	Application of specified conductive layer (EPO)

E21.084	Treatment of complete device, e.g., electroforming, heat treating (EPO)	E21.101Using reduction or decomposition of gaseous compound yielding solid
E21.085	Device having semiconductor body comprising Group IV elements or Group III-V compounds with or without impurities, e.g., doping materials (EPO)	condensate, i.e., chemical deposition (EPO) E21.102Epitaxial deposition of Group IV elements, e.g., Si, Ge, C (EPO) E21.103Deposition on a
	<pre>Intermixing or interdiffusion or disordering of Group III-V heterostructures, e.g., IILD (EPO)</pre>	semiconductor substrate which is different from the semiconductor material being deposited, i.e., formation of
	Joining of semiconductor body for junction formation (EPO)	heterojunctions (EPO) E21.104Deposition on an
	<pre>By direct bonding (EPO)Multistep processes for</pre>	<pre>insulating or a metallic substrate (EPO)</pre>
	manufacture of device using quantum interference effect,	E21.105Epitaxial deposition of diamond (EPO)
	e.g., electrostatic Aharonov- Bohm effect (EPO)	E21.106Doping during the epitaxial deposition (EPO)
E21.09	Deposition of semiconductor material on substrate, e.g., epitaxial growth, solid phase	E21.107Deposition of diamond (EPO) E21.108Epitaxial deposition of Group III-V compound (EPO)
₽ 21 ∩01	epitaxy (EPO)Using physical deposition,	E21.109Using molecular beam
E21.091	e.g., vacuum deposition, sputtering (EPO)	technique (EPO) E21.11Doping the epitaxial deposit (EPO)
	Epitaxial deposition of Group IV element, e.g., Si, Ge (EPO)	E21.111Doping with transition metals to form semi-insulating layers (EPO)
E21.093	Deposition on semiconductor substrate being different from deposited semiconductor material; i.e., formation of heterojunctions	E21.112Deposition on a semiconductor substrate not being Group III-V compound (EPO)
F21 N94	(EPO)Deposition on insulating	E21.113Deposition on an insulating or a metallic
	or meta llic substrate (EPO)Epitaxial deposition of	substrate (EPO) E21.114Using liquid deposition
	diamond (EPO)	(EPO) E21.115Epitaxial deposition of
	Deposition of diamond (EPO)Epitaxial deposition of	Group IV elements, e.g., Si, Ge, C (EPO)
	Group III-V compound (EPO)Deposition on semiconductor substrate not being an Group III-V compound (EPO)	E21.116Deposition on a semiconductor substrate which is different from the semiconductor material being deposited, i.e., formation of
E21.099	Deposition on insulating or metallic substrate (EPO)	heterojunction (EPO) E21.117Epitaxial deposition of
E21.1	Doping during epitaxial deposition (EPO)	Group III-V compound (EPO) E21.118Deposition on a
	acposition (Ero)	semiconductor substrate not being an Group III-V compound (EPO)

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E21.119Characterized by the substrate (EPO)	E21.134Using a coherent energy beam, e.g., laser or electron
E21.12Characterized by the post-	beam (EPO)
treatment used to control the	E21.135Diffusion of impurity
interface betw een substrate	material, e.g., doping
and epitaxial layer, e.g., ion	material, electrode material,
implantation followed by	into or out of a semiconductor
annealing (EPO)	body, or between semiconductor
E21.121Substrate is crystalline	regions; interactions between
	two or more impurities;
insulating material, e.g.,	<u>-</u>
sapphire (EPO)	redistribution of impurities
E21.122Bonding of semiconductor	(EPO)
wafer to insulating substrate	E21.136From the substrate during
or to semic onducting	epitaxy, e.g., autodoping;
substrate using an	preventing or using autodoping
intermediate insulating layer	(EPO)
	E21.137To control carrier lifetime,
(EPO)	
E21.123Substrate is crystalline	i.e., deep level dopant (EPO)
semiconductor material, e.g.,	E21.138In Group III-V compound
lattice adaptation,	(EPO)
heteroepitaxy (EPO)	E21.139Lithium-drift (EPO)
E21.124Heteroepitaxy (EPO)	E21.14Diffusion source (EPO)
E21.125Defect and dislocati on	E21.141Using diffusion into or out
suppression due to lattice	of a solid from or into a
mismatch, e.g., lattice	gaseous phase (EPO)
adaptation (EPO)	E21.142Diffusion into or out of
E21.126Group III-V compound on	
	Group III-V compound (EPO)
dissimilar Group III-V	E21.143From or into plasma phase
compound (EPO)	(EPO)
E21.127Group III-V compound on	E21.144Using diffusion into or out
Si or Ge (EPO)	of a s olid from or into a
E21.128Carbon on a noncarbon	solid phase, e.g., a doped
semiconductor substrate (EPO)	oxide layer (EPO)
E21.129Group IVA, e.g., Si, C, Ge	E21.145Diffusion into or out of
on Group IVB, e.g., Ti, Zr	Group IV semiconductor (EPO)
(EPO)	-
E21.13The substrate is	E21.146Using predeposition of
	impurities into the
crystalline conducting	semiconductor surface, e.g.,
material, e.g., metallic	from gaseous phase (EPO)
silicide (EPO)	E21.147By ion implantation (EPO)
E21.131Selective epilaxial growth,	E21.148From or through or into an
e.g., simultaneous deposition	applied layer, e.g.,
of mono- and non-mono	photoresist, nitride (EPO)
semiconductor material (EPO)	E21.149Applied layer is oxide,
E21.132Preparation of substrate	e.g., P 2 0 5 , PSG, H 3 BO 3 ,
for selective epitaxy (EPO)	doped oxide (EPO)
E21.133Epitaxial re-growth of non-	E21.15Through the applied
monocrystalline semiconductor	
material, e.g., lateral	layer (EPO)
	E21.151Applied layer being
epitaxy by seeded solidific	silicon or silicide or SIPOS,
ation, solid-state	e.g., polysilicon, porous
crystallization, solid-state	silicon (EPO)
graphoepitaxy, explosive	E21.152Diffusion into or out of
crystallization, grain growth	Group III-V compound (EPO)
in polycrystalline material	

(EPO)

E21.153Using diffusion into or out of a solid from or into a	E21.172On semiconductor body comprising Group III-V
liquid phase, e.g., alloy	compound (EPO)
diffusion process (EPO)	E21.173Deposition of Schottky
E21.154Alloying of impurity	electrode (EPO)
material, e.g., doping	E21.174From a liquid, e.g.,
material, electrode material,	electrolytic deposition (EPO)
with a semiconductor body	E21.175Using an external
(EPO)	electrical current, i.e.,
E21.155Alloying of doping material	electro-deposition (EPO)
with Group III-V compound	E21.176Manufacture or post-
(EPO)	treatment of electrode having
E21.156Alloying of electrode	a capacitive structure, i.e.,
material (EPO)	gate structure for field-
E21.157With Group III-V compound	effect device (EPO)
(EPO)	E21.177MOS-gate structure (EPO)
E21.158Manufacture of electrode on	E21.177Joint-gate structure (EPO)
semiconductor body using	
process other than by	E21.179Floating or plural gate
epitaxial growth, diffusion of	structure (EPO)
impurities, alloying of	E21.18Gate structure with
impurity materials, or	charge-trapping insulator
radiation bombardment (EPO)	(EPO)
E21.159Deposition of conductive or	E21.181On semiconductor body not
insulating material for	comprising Group IV element,
electrode conducting electric	e.g., Group III-V compound
current (EPO)	(EPO)
	E21.182On semiconductor body
E21.16From a gas or vapor, e.g., condensation (EPO)	comprising Group IV element
	excluding non-elemental Si,
E21.161Of conductive layer (EPO)	e.g., Ge, C, diamond, silicon
E21.162On semiconductor body	compound or compound, such as
comprising Group IV element	SiC or SiGe (EPO)
(EPO)	E21.183For charge-coupled device
E21.163Deposition of Schottky	(EPO)
electrode (EPO)	E21.184PN-homojunction gate
E21.164 0 layer comprising	structure (EPO)
silicide (EPO)	E21.185For charge-coupled device
E21.165Conductive layer	(EPO)
comprising silicide (EPO)	E21.186Schottky gate structure
E21.166Conductive layer	(EPO)
comprising semiconducting	E21.187For charge-coupled device
material (EPO)	(EPO)
E21.167Making of side-wall	E21.188Heterojunction gate
contact (EPO)	structure (EPO)
E21.168Conductive layer	E21.189For charge-coupled device
comprising transition metal,	(EPO)
e.g., Ti, W, Mo (EPO)	E21.19Making electrode structure
E21.169By physical means, e.g.,	comprising conductor-
sputtering, evaporation (EPO)	insulator-semiconductor, e.g.,
E21.17By chemical means, e.g.,	MIS gate (EPO)
CVD, LPCVD, PECVD, laser CVD	E21.191Insulator formed on silicon
(EPO)	semiconductor body (EPO)
E21.171Selective deposition	E21.192Characterized by insulator
(EPO)	(EPO)

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E21.193	On single crystalline silicon (EPO)	E21.206Lithography, isolation, or planarization-related
	Characterized by treatment after formation of definitive gate conductor (EPO)	aspects of making conductor- insulator-semiconductor structure, e.g., sub- lithography lengths; to solve problems arising at crossing
	Characterized by conductor (EPO)Final conductor next to	with side of device isolation (EPO)
E21.190	insulator having lateral composition or doping variation, or being formed laterally by more than one deposition step (EPO)	E21.207Insulator formed on nonelemental silicon semiconductor body, e.g., Ge, SiGe, SiGeC (EPO) E21.208Comprising layer having
	next to insulator being silicon e.g., polysilicon, with or without impurities (EPO)	ferroelectric properties (EPO) E21.209Making electrode structure comprising conductor- insulator-conuctor-insulator- semiconductor, e.g., gate
E21.198	Conductor comprising at least another nonsilicon conductive layer (EPO)	stack for non-volatile memory (EPO) E21.21Comprising charge trapping
E21.199		insulator (EPO) E21.211Treatment of semiconductor body using process other than deposition of semiconductor
E21.2	Conductor comprising metal or metallic silicide formed by deposition e.g., sputter deposition, i.e.,	material on a substrate, diffusion or alloying of impurity material, or radiation treatment (EPO)
E21.201	without silicidation reaction (EPO)Conductor layer next to	E21.212Hydrogenation or deuterization, e.g., using atomic hydrogen or deuterium
T01 000	insulator is Si or Ge or C and their non-Si alloys (EPO)	from a plasma (EPO) E21.213Of Group III-V compound (EPO)
E21.202	Conductor layer next to the insulator is single metal, e.g., Ta, W, Mo, Al (EPO)	E21.214To change their surface- physical characteristics or
E21.203	Conductor layer next to insulator is metallic silicide (Me Si) (EPO)	shape, e.g., etching, polishing, cutting (EPO) E21.215Chemical or electrical
E21.204		<pre>treatment, e.g., electrolytic etching (EPO) E21.216Electrolytic etching (EPO)</pre>
E21.205	composite or compound, e.g., TiN (EPO)Characterized by	E21.217Of Group III-V compound (EPO)
	sectional shape, e.g., T-shape, inverted T, spacer (EPO)	E21.218Plasma etching; reactive- ion etching (EPO) E21.219Chemical etching (EPO) E21.22Etching of Group III-V compound (EPO)
		E21.221Anisotropic liquid etching (EPO)
		E21.222Vapor phase etching (EPO)

	Anisotropic liquid etching (EPO)	E21.245	Removal by chemical etching, e.g., dry etching
	Chemical cleaning (EPO)Cleaning diamond or graphite (EPO)	E21.246	(EPO)Removal by selective chemical etching, e.g.,
	Dry cleaning (EPO)	F21 247	<pre>selective dry etching through mask (EPO)Doping insulating layer</pre>
E21.228	fluoride (HF) (EPO)Wet cleaning only (EPO)		(EPO)
E21.229	Combining dry and wet cleaning steps (EPO)		By ion implantation (EPO)
E21.23	<pre>With simultaneous mechanical treatment, e.g., chemical-mechanical polishing</pre>		by chemical or physical means (EPO)
m01 001	(EPO)	E21.25	Etching inorganic layer
	Using mask (EPO)	₽21 251	(EPO)
E21.232	Characterized by their		By chemical means (EPO)By dry-etching (EPO)
	composition, e.g., multilayer		Of layers not
E21.233	<pre>masks, materials (EPO)Characterized by their size, orientation,</pre>	EZI.ZJJ	containing Si, e.g., PZT, Al 2 O 3 (EPO)
	disposition, behavior, shape, in horizontal or vertical	E21.254	Etching organic layer (EPO)
	plane (EPO)	E21.255	By chemical means (EPO)
E21.234	Characterized by their	E21.256	By dry-etching (EPO)
	behavior during process, e.g.,	E21.257	Using mask (EPO)
	soluble mask, redeposited mask	E21.258	Using masks (EPO)
E21.235	(EPO)Characterized by process	E21.259	<pre>Organic layers, e.g., photoresist (EPO)</pre>
	involved to create mask, e.g., lift-off mask, sidewall, or to	E21.26	Layer comprising organo- silicon compound (EPO)
	<pre>modify the mask, e.g., pre- treatment, post-treatment</pre>	E21.261	Layer comprising polysiloxane compound (EPO)
T01 026	(EPO)	E21.262	Layer comprising
E21.236	Process specially		hydrogen silsesquioxane (EPO)
	adapted to improve resolution of mask (EPO)	E21.263	Layer comprising silazane compounds (EPO)
E21.237	Mechanical treatment, e.g.,	E21.264	Layers comprising fluoro
	grinding, polishing, cutting (EPO)		hydrocarbon compounds, e.g., polytetrafluoroethylene (EPO)
E21.238	<pre>Making grooves, e.g., cutting (EPO)</pre>	E21.265	By Langmuir-Blodgett technique (EPO)
E21.239	Using abrasion, e.g.,	E21.266	Inorganic layer (EPO)
E 01 04	sand-blasting (EPO)	E21.267	Composed of alternated
E21.24	<pre>To form insulating layer thereon, e.g., for masking or by using photolithographic</pre>		layers or of mixtures of nitrides and oxides or of oxynitrides, e.g., formation
	technique (EPO)		of oxynitride by oxidation of
	Post-treatment (EPO)		nitride layer (EPO)
	Of organic layer (EPO)	E21.268	Of silicon (EPO)
E21.243	Planarization of insulating layer (EPO)	E21.269	Formed by deposition
E21.244	Involving dielectric	⊡ 21 27	from a gas or vapor (EPO)
· -	removal step (EPO)	E21.27	Carbon layer, e.g., diamond-like layer (EPO)

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E21.271	Composed of oxide or glassy oxide or oxide based glass (EPO)	E21.294 .	Deposition/post-treatment of noninsulating, e.g., conductive - or resistive -
E21.272	With perovskite structure (EPO)		layers on insulating layers (EPO)
E21.273	<pre>Deposition of porous oxide or porous glassy oxide or oxide based porous glass (EPO)</pre>		Deposition of layer comprising metal, e.g., metal, alloys, metal compounds (EPO)Of metal-silicide layer
E21.274	Deposition from gas or vapor (EPO)		(EPO)Deposition of
E21.275	Deposition of boron or phosphorus doped silicon oxide, e.g., BSG, PSG, BPSG (EPO)		semiconductive layer, e.g., poly - or amorphous silicon layer (EPO)Deposition of
E21.276	Deposition of halogen		superconductive layer (EPO)
	<pre>doped silicon oxide, e.g., fluorine doped silicon oxide (EPO)</pre>	E21.299 .	Deposition of conductive or semi-conductive organic layer (EPO)
E21.277	Deposition of carbon	E21.3 .	Post treatment (EPO)
	<pre>doped silicon oxide, e.g., SiOC (EPO)</pre>		Oxidation of silicon- containing layer (EPO)
E21.278	Deposition of silicon oxide (EPO)		Nitriding of silicon- containing layer (EPO)
E21.279	On silicon body (EPO)	E21.303 .	Planarization (EPO)
E21.28	Deposition of aluminum oxide (EPO)	E21.304 .	By chemical mechanical polishing (CMP) (EPO)
E21.281	On a silicon body (EPO)	E21.305 .	Physical or chemical etching of layer, e.g., to
	Formed by oxidation (EPO)Of semiconductor		<pre>produce a patterned layer from pre-deposited extensive layer (EPO)</pre>
121.203	material, e.g., by oxidation of semiconductor body itself	E21.306 .	By physical means only (EPO)
F21 284	(EPO)By thermal oxidation	E21.307 .	Of silicon-containing layer (EPO)
	(EPO)Of silicon (EPO)	E21.308 .	By chemical means only
		ED1 200	(EPO)
	Of Group III-V compound (EPO)		By liquid etching only (EPO)
	By anodic oxidation (EPO)	E21.31 .	By vapor etching only (EPO)
E21.288	Of silicon (EPO)	E21.311 .	Using plasma (EPO)
E21.289	Of Group III-V compound (EPO)	E21.312 .	Of silicon-containing layer (EPO)
E21.29	<pre>e.g., Al deposited on body, e.g., formation of multi-layer insulating structures (EPO)</pre>		Pre- or post- treatment, e.g., anti- corrosion process (EPO) Using mask (EPO)
E21.291	By anodic oxidation (EPO)	E21.315 .	Doping layer (EPO)
E21.292	(EPO)Inorganic layer composed of nitride (EPO)	E21.316 .	Doping polycrystalline or amorphous silicon layer (EPO)
E21.293	Of silicon nitride (EPO)		\ /

E21.317	To modify their internal properties, e.g., to produce	E21.34	In Group III-V compound (EPO)
E21.318	<pre>internal imperfections (EPO)Of silicon body, e.g., for</pre>	E21.341	Of electrically active species (EPO)
	gettering (EPO)	E21.342	\ldots Through-implantation
E21.319	Using cavities formed by		(EPO)
	inert gas ion implantation,	E21.343	Characterized by the
	e.g., hydrogen, noble gas		implantation of both
	(EPO)		electrically active and
E21.32	Of silicon on insulator		inactive species in the same
	(SOI) (EPO)		semiconductor region to be
E21.321	Thermally inducing defects		doped (EPO)
	using oxygen present in	E21.344	In diamond (EPO)
	silicon body for intrinsic	E21.345	Characterized by the angle
	gettering (EPO)		between the ion beam and the
E21.322	Of Group III-V compound,		crystal planes or the main
	e.g., to make them semi-		crystal surface (EPO)
	insulating (EPO)	E21.346	Using mask (EPO)
E21.323	Of diamond body (EPO)	E21.347	Using electromagnetic
	Thermal treatment for		radiation, e.g., laser
	modifying the properties of		radiation (EPO)
	semiconductor body, e.g.,	E21.348	Using X-ray laser (EPO)
	annealing, sintering (EPO)	E21.349	Using incoherent radiation
E21.325	For the formation of PN		(EPO)
	junction without ad dition of	E21.35	Multi-step process for
	impurities (EPO)		manufacture of device of
E21.326	Of Group III-V compound		bipolar type, e.g., diodes,
	(EPO)		transistors, thyristors,
E21.327	Application of electric		resistors, capacitors) (EPO)
	current or field, e.g., for	E21.351	Device comprising one or two
	electroforming (EPO)		electrodes, e.g., diode,
E21.328	Radiation treatment (EPO)		resistor or capacitor with PN
E21.329	Using natural radiation,		or Schottky junctions (EPO)
	e.g., alpha , beta or gamma	E21.352	Diode (EPO)
	radiation (EPO)	E21.353	Tunnel diode (EPO)
E21.33	To produce chemical element	E21.354	Transit time diode, e.g.,
	by transmutation (EPO)		IMPATT, TRAPATT diode (EPO)
E21.331	With high-energy radiation	E21.355	Break-down diode, e.g.,
	(EPO)		Zener diode, avalanche diode
E21.332	For etching, e.g., sputter		(EPO)
	etching (EPO)	E21.356	Zener diode (EPO)
E21.333	For heating, e.g., electron	E21.357	Avalanche diode (EPO)
	beam heating (EPO)	E21.358	Rectifier diode (EPO)
E21.334	Producing ions for	E21.359	Schottky diode (EPO)
	implantation (EPO)	E21.36	Planar diode (EPO)
E21.335	In Group IV semiconductor	E21.361	Multi-layer diode, e.g.,
	(EPO)		PNPN or NPNP diode (EPO)
E21.336	Of electrically active	E21.362	Gat ed-diode structure,
	species (EPO)		e.g., SITh, FCTh, FCD (EPO)
E21.337	Through-implantation	E21.363	Resistor with PN junction
	(EPO)		(EPO)
E21.338	Recoil-implantation (EPO)	E21.364	Capacitor with PN - or
E21.339	Of electrically inactive		Schottky junction, e.g.,
	species in silicon to make		varactor (EPO)
	buried insulating layer (EPO)		

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	Active layer is Group III-V compound (EPO)	E21.39	Structurally associated with other devices (EPO)
E21.366	Diode (EPO)	E21.391	Other device being a
	With an heterojunction,		controlling device of the
EZI.507			field-effect-type (EPO)
	e.g., resonant tunneling	T01 200	
	diodes (RTD) (EPO)	E21.392	Bi-directional thyristor
	Schottky diode (EPO)		(EPO)
E21.369	Device comprising three or	E21.393	Active layer is Group III-
	more electrodes (EPO)		V compound (EPO)
E21.37	Transistor (EPO)	E21.394	Multi-step process for the
E21.371	Heterojunction transistor		manufacture of unipolar device
	(EPO)		(EPO)
E01 270	Bipolar thin film	E21 395	Transistor-like structure,
EZI.3/Z		HZ1.373	e.g., hot electron transistor
B01 2B2	transistor (EPO)		(HET); metal base transistor
	Lateral transistor (EPO)		•
E21.374	Schottky transistor (EPO)		(MBT); resonant tunneling HET
E21.375	Silicon vertical		(RHET); resonant tunneling
	transistor (EPO)		transistor (RTT); bulk
E21.376	Planar transistor (EPO)		<pre>barrier transistor (BBT);</pre>
	Mesa-planar transistor		planar doped barrier
	(EPO)		transistor (PDBT); charge
F21 378	Inverse transistor (EPO)		<pre>injection transistor (CHINT);</pre>
	With single crystalline		ballistic transistor (EPO)
EZI.3/9		E21.396	Metal-insulator-
	emitter, collector or base		semiconductor capacitor, e.g.,
	including extrinsic, link or		trench capacitor (EPO)
	graft base formed on th e	E21.397	Comprising PN junction,
	silicon substrate, e.g., by		e.g., hybrid capacitor (EPO)
	epitaxy, recrystallization,	F21 398	Active layer is Group III-V
	after insulating device	HZ1.370	compound (EPO)
	isolation (EPO)	по1 200	-
E21.38	Where main current goes	EZI.399	Transistor-like structure,
	through whole of silicon		e.g., hot electron transistor
	substrate, e.g., power bipolar		(HET), metal base transistor
	transistor (EPO)		(MBT), resonant tunneling hot
E21.381	With a multi- emitter,		electron transistor (RHET),
	e.g., interdigitated,		resonant tunneling transistor
	multicellular, distributed		(RTT), bulk barrier transistor
	(EPO)		(BBT), planar doped barrier
F21 382	Field-effect controlled		transistor (PDBT), charge
HZ1.50Z	bipolar-type transi stor,		injection transistor (CHINT)
			(EPO)
	e.g., insulated gate bipolar	E21.4	Field-effect transistor
501 202	transistor (IGBT) (EPO)		(EPO)
E21.383	Vertical insulated gate	E21.401	Using static field induced
	bipolar transistor (EPO)		region, e.g., SIT, PBT (EPO)
E21.384	With recessed gate (EPO)	F21 402	Permeable base transistor
E21.385	With recess formed by	121.102	(PBT) (EPO)
	etching in source/emitter	₽O1 4∩⊃	With heterojunction
	contact region (EPO)	£∠⊥.4U3	
E21.386	Active layer, e.g., base,		interface channel or gate,
	is Group III-V compound (EPO)		e.g., HFET, HIGFET, SISFET,
E21.387			HJFET, HEMT (EPO)
	(EPO)		
F21 200			
	Thyristor (EPO)		
±∠⊥.389	Lateral or planar		
	thyristor (EPO)		

E21.404	With one or zero or quasi- one or quasi-zero dimensional	E21.42	With recess formed by etching in source/base contact
	charge carrier gas channel,		region (EPO)
E21 405	<pre>e.g., quantum wire FET; single electron trans istor (SET); striped channel transistor; coulomb blockade device (EPO)Active layer is Group III-V</pre>	E21.421	With multiple gate, one gate having MOS structure and others having same or a different structure, i.e., non MOS, e.g., JFET gate (EPO)
HZ1.105	compound, e.g., III-V velocity modulation transistor (VMT),		With floating gate (EPO)With charge trapping gate
	NERFET (EPO)	121.123	insulator, e.g., MNOS
E21.406	Using static field induced		transistor (EPO)
E21.407	region, e.g., SIT, PBT (EPO)With an heterojunction	E21.424	Lateral single gate silicon transistor (EPO)
	<pre>interface channel or gate, e.g., HFET, HIGFET, SI SFET, HJFET, HEMT (EPO)</pre>	E21.425	With source or drain region formed by Schottky
E21.408	With one or zero or quasi- one or quasi-zero dimensional		<pre>barrier or conductor- insulator-semiconductor structure (EPO)</pre>
	channel, e.g., in plane gate transistor (IPG), single electron transistor (SET),	E21.426	With single crystalline channel formed on the silicon substrate after insulating
	striped channel transistor, coulomb blockade device (EPO)	E01 40E	device isolation (EPO)
E21.409	With an insulated gate (EPO)	E21.42/	With asymmetry in channel direction, e.g., high-voltage lateral transistor with
	Vertical transistor (EPO)		channel containing layer,
E21.411	Thin film unipolar	E01 400	e.g., p-base (EPO)
E21.412	transistor (EPO)Amorphous silicon or	EZ1.428	With a recessed gate, e.g., lateral U-MOS (EPO)
	polysilicon transistor (EPO)	E21.429	
E21.413	Lateral single gate single channel transistor with noninverted structure, i.e., channel layer is formed before gate (EPO)	E21.43	recess at gate location (EPO)Recessing gate by adding semiconductor material at source (S) or drain (D) location, e.g., transist or
E21.414	Lateral single gate single channel transistor with		with elevated single crystal S and D (EPO)
	<pre>inverted structure, i.e., channel layer is formed after gate (EPO)</pre>	E21.431	With source and drain recessed by etching or recessed and refi lled (EPO)
	<pre>Monocrystalline silicon transistor on insulating substrate, e.g., quartz substrate (EPO)</pre>	E21.432	With source and drain contacts formation strictly before final gate formation, e.g., contact first technology
E21.416	On sapphire substrate,	-01 400	(EPO)
E21.417	<pre>e.g., silicon on sapphire (SOS) transistor (EPO)With channel containing layer, e.g., p-base, fo rmed</pre>	E21.433	Where the source and drain or source and drain extensions are self-aligned to sides of gate (EPO)
	in or on drain region, e.g.,	E21.434	With initial gate mask
E21.418	DMOS transistor (EPO)Vertical power DMOS transistor (EPO)		or masking layer complementary to prospective gate location, e.g., with dummy source and
E21.419			drain contacts (EPO)

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E21.435Lateral single gate single channel silicon transistor with both lightly doped source and drain extensions and source and drain self-aligned to sides of gate, e.g., LDD MOSFET (EPO) E21.436Gate comprising layer with ferroelectric properties (EPO) E21.437With lightly doped drain self-caligned selective properties (EPO) E21.438Using self-aligned silicidation, i.e., salicide (EPO) E21.449Providing different silicide thicknesses on gate and on source or drain (EPO) E21.441Esing self-aligned selective metal deposition simultaneously on gate and on source or drain (EPO) E21.442With gate at side of solute hrough stopper or threshold implant under gate region (EPO) E21.444Wing self-aligned punch through stopper or threshold implant under gate region (EPO) E21.445With PN junction or heterojunction gate (EPO) E21.446With provided (EPO) E21.447Vertical transistor, e.g., teenetrons (EPO) E21.448With hemojunction gate (EPO) E21.449	по1 42E		TO1 454	Danas and America Fig. 1
two or more independent t gates E21.436Gate comprising layer with E21.437With lightly doped drain selectively formed at side of gate (EPO) E21.438Wising self-aligned silicidation, i.e., salicide (EPO) E21.439Providing different silicide thicknesses on gate and on source or drain (EPO) E21.441Vising self-aligned selective metal deposition simultaneously on gate and on source or drain (EPO) E21.442With gate at side of channel (EPO) E21.443Wising self-aligned punch through stopper or threshold implant under gate region (EPO) E21.444Using dummy gate wherein at least part of final gate is self-aligned to dummy gate (EPO) E21.445With PN junction or heterojunction gate (EPO) E21.446With PN homojunction gate (EPO) E21.447Wertical transistor, e.g., tecnetrons (EPO) E21.448With heterojunction gate (EPO) E21.449Active layer is Group III- V compound (EPO) E21.449With PN homojunction gate (EPO) E21.441Active layer is Group III- V compound (EPO) E21.442With heterojunction gate (EPO) E21.443With heterojunction gate (EPO) E21.444With heterojunction gate (EPO) E21.445With Schottky gate, e.g., Lateral single-gate transistors (EPO) E21.446Using diffusion into or out of solid from or into gaseous phase (EPO) E21.451Wative layer being Group III-V compound (EPO) E21.446Using preduction or decomposition of gaseous compound or alloy, e.g., liquid plase epitaxy (EPO) E21.467Using diffusion into or out of solid from or into gaseous phase (EPO) E21.468Using diffusion into or out of solid from or into gaseous of solid from or into solid phase, e.g., dopent, electrode material, e.g., dopant, electrode material, with semiconductor body (pED) E21.462Using production or decomposition of gaseous compound yielding solid condensate, i.e., chemical deposition (PEO) E21.465Using diffusion into or out of solid from or into gase out of solid from or into solid phase, e.g., do	E21.435	channel silicon transistor with both lightly doped source and drain extensions and	E21.454	gate is made before formation, e.g., activation anneal, of source and drain regions in
ferroelectric properties (EPO) E21.437With lightly doped drain selectively formed at side of gate (EPO) E21.438With shorthry gate (EPO) E21.439Providing different silicide thicknesses on gate and on source or drain (EPO) E21.449Using self-aligned selective metal deposition simultaneously on gate and on source or drain (EPO) E21.441With gate at side of channel (EPO) E21.442With gate at side of channel (EPO) E21.443Using gate-aligned punch through stopper or threshold implant under gate region (EPO) E21.444Using dummy gate wherein at least part of final gate (EPO) E21.445With PN homojunction gate (EPO) E21.446With PN homojunction gate (EPO) E21.447With PN homojunction gate (EPO) E21.448With PN homojunction gate (EPO) E21.449Active layer is Group III-v compound (EPO) E21.451With Schottky gate, e.g., dopant, electrode material, into or out of solid from or into solid phase, e.g., alogy diffusion process (EPO) E21.452With Schottky gate, e.g., dopant, electrode material, with spate (EPO) E21.453Share (EPO) E21.456With Schottky gate (EPO) E21.459Evice having semiconductor body of without impurity semiconductor body of without impurities, e.g., doping materials (EPO) E21.461Deposition of semiconductor material on substrate, e.g., epitaxial growth (EPO) E21.462Using physical deposition, e.g., vacuum deposition, sputtering (EPO) E21.463Using in reduction or decomposition of gaseous compound yielding solid condensate, i.e., chemical deposition (EPO) E21.464Using in reduction or decomposition of gaseous compound yielding solid condensate, i.e., chemical deposition (EPO) E21.465Charge tanking capt (EPO) E21.459Device having semiconductor body (EPO) E21.450With Schottky and the process (EPO) E21.461Deposition of semiconductor body (EPO) E21.462Using physical deposition (EPO) E21.463Using liquid deposition (EPO) E21.464Usin	E21 426	MOSFET, DDD MOSFET (EPO)	E21.455	two or more independen t gates
E21.437With lightly doped drain selectively formed at side of gate (EPO) E21.438Using self-aligned silicidation, i.e., salicide (EPO) E21.439Providing different silicide thicknesses on gate and on source or drain (EPO) E21.441With self-aligned selective metal deposition simultaneously on gate and on source or drain (EPO) E21.442With gate at side of channel (EPO) E21.443Using self-aligned punch through stopper or threshold implant under gate region (EPO) E21.444Using self-aligned punch through stopper or threshold implant under gate region (EPO) E21.445With PN homojunction gate (EPO) E21.446With PN homojunction gate (EPO) E21.447Vertical transistor, e.g., c.g., c.e.ceterons (EPO) E21.448With Schottky gate, e.g., alloyed diffusion into or out of semiconductor regions (EPO) E21.452With Schottky gate e.g., dummy-gate process (EPO) E21.453Verces wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) E21.453Vith schottky gate, e.g., dummy-gate process (EPO) E21.454With schottky gate, e.g., dummy-gate process (EPO) E21.455With schottky gate, e.g., dummy-gate process (EPO) E21.457With Schottky gate, e.g., dopant, electrode material, e.g., dopant, electrode material, into or out of solid from or into gate (EPO) E21.458With Schottky gate, e.g., alloying of impurity material, e.g., dopant, electrode material, with semiconductor body (EPO) E21.459With Schottky gate, e.g., alloy diffusion process (EPO) E21.461With Schottky gate, e.g., alloying of impurity material, e.g., dopant, electrode material, with semiconductor body (EPO)	E21.430		E21.456	
E21.438Using self-aligned silicidation, i.e., salicide (EFO) E21.439Providing different silicide thicknesses on gate and on source or drain (EFO) E21.441Using self-aligned selective metal deposition simultaneously on gate and on source or drain (EFO) E21.442With gate at side of channel (EFO) E21.443Using self-aligned punch through stopper or threshold implant under gate region (EFO) E21.444Using dummy gate wherein at least part of final gate is self-aligned to dummy gate (EFO) E21.445With PN junction or heterojunction gate (EFO) E21.446With PN homojunction gate (EFO) E21.447Vertical transistor, e.g., tecnetrons (EFO) E21.448With PN homojunction gate (EFO) E21.449Active layer is Group III- V compound (EPO) E21.451Active layer is Group III- V compound (EPO) E21.452With Schottky gate, e.g., MESFET (EPO) E21.453Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EFO) E21.453Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EFO) E21.453Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EFO)	E21.437	selectively formed at side of	E21.457 E21.458	With insulated gate (EPO)With Schottky gate (EPO)
E21.439Providing different silicide thicknesses on gate and on source or drain (EPO) E21.441Using self-aligned selective metal deposition simultaneously on gate and on source or drain (EPO) E21.441Active layer is Group III-V compound (EPO) E21.442With gate at side of channel (EPO) E21.443Using self-aligned punch through stopper or threshold implant under gate region (EPO) E21.444Using dummy gate wherein at least part of final gate is self-aligned to dummy gate (EPO) E21.445With PN junction or heterojunction gate (EPO) E21.447Vertical transistor, e.g., tecnetrons (EPO) E21.449With PN homojunction gate (EPO) E21.449With Schottky gate, e.g., mESFET (EPO) E21.451Active layer being Group III-V compound (EPO) E21.452Lateral single-gate transistors (EPO) E21.453Process wherein final gate is smade after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) E21.451Process wherein final gate is smade after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) E21.452Sing physical deposition of genteration (EPO) E21.463Using preduction or decomposition of gaseous compound yielding solid condensate, i.e., chemical deposition (EPO) E21.464Using liquid deposition (EPO) E21.465From molten solution of compound or alloy, e.g., liquid phase epitaxy (EPO) E21.466Using deposition or decomposition of gaseous compound or gate (EPO) E21.461Deposition of semiconductor material on substrate, e.g., deposition, e.g., vacuum deposition, e.g., vacuum deposition of decomposition of gaseous compound yielding solid condensate, i.e., chemical deposition (EPO) E21.465From molten solution of compound or alloy, e.g., liquid phase epitaxy (EPO) E21.466Using diffusion into or out of solid from or into solid phase, e.g., dopend oxide layer (EPO) E21.467Using diffusion into or out of solid from or into solid phase, e.g., dopend oxide l	E21.438	Using self-aligned silicidation, i.e., salicide	621.439	body other than carbon, Si, Ge, SiC, Se, Te, Cu 2 O, CuI,
E21.44Using self-aligned selective metal deposition simultaneously on gate and on source or drain (EPO) E21.441Active layer is Group III- V compound (EPO) E21.442With gate at side of channel (EPO) E21.443Using self-aligned punch through stopper or threshold implant under gate region (EPO) E21.444Using dummy gate wherein at least part of final gate is self-aligned to dummy gate (EPO) E21.445With PN junction or heterojunction gate (EPO) E21.446With PN thomojunction gate (EPO) E21.447Vertical transistor, e.g., tecnetrons (EPO) E21.448With heterojunction gate (EPO) E21.449Active layer is Group III- V compound (EPO) E21.451Active layer being Group III- V compound (EPO) E21.452Lateral single-gate transistors (EPO) E21.453Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) E21.453Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) E21.453Sing self-aligned punch through stopper or threshold implant under gate as ide of channel (EPO) E21.462Using physical deposition, e.g., vacuum deposition of decomposition of gaseous compound vielding solid condensate, i.e., chemical deposition (EPO) E21.465Using physical deposition of e.g., vacuum deposition (EPO) E21.465Using physical deposition of compound or alloy, e.g., liquid phase epitaxy (EPO) E21.466Using diffusion into or out of solid from or into or out of solid from or into liquid phase, e.g., alloy diffusion pro	E21.439	silicide thicknesses on gate	TO1 46	or without impurities, e.g., doping materials (EPO)
Source or drain (EPO) E21.441Active layer is Group III-V compound (EPO) E21.442With gate at side of channel (EPO) E21.443Using self-aligned punch through stopper or threshold implant under gate region (EPO) E21.444Using dummy gate wherein at least part of final gate is self-aligned to dummy gate (EPO) E21.445With PN junction or heterojunction gate (EPO) E21.446With PN homojunction gate (EPO) E21.447Vertical transistor, e.g., teenetrons (EPO) E21.448With heterojunction gate (EPO) E21.449Active layer is Group III-V compound (EPO) E21.451Active layer is Group III-V compound (EPO) E21.452Lateral single-gate transistors (EPO) E21.453Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) E21.451Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) E21.452Lateral single-gate transistors (EPO) E21.453Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) E21.453Vertical transistor, (EPO) E21.454Vertical transistor, (EPO) E21.455With PN homojunction gate (EPO) E21.456Sing physical deposition, sputtering (EPO) E21.463Using reduction or decompound in of gaseous compound yielding solid condensate, i.e., chemical deposition (EPO) E21.464Using liquid deposition (EPO) E21.465From molten solution of compound or alloy, e.g., liquid phase epitaxy (EPO) E21.466From molten solution of compound or alloy, e.g., liquid phase epitaxy (EPO) E21.467Sing diffusion into or out of solid from or into gate (EPO) E21.468Sing diffusion into or out of solid from or into solid phase, e.g., alloy diffusion process (EPO) E21.470Sing diffusion into or out of solid from or into solid phase, e.g., alloy diffusion process (EPO) E21.471Active layer is Grou	E21.44	Using self-aligned selective metal deposition		Deposition of semiconductor material on substrate, e.g.,
E21.442With gate at side of channel (EPO) E21.443Using self-aligned punch through stopper or threshold implant under gate region (EPO) E21.444Using dummy gate wherein final gate is self-aligned to dummy gate (EPO) E21.445With PN junction or heterojunction gate (EPO) E21.446With PN homojunction gate (EPO) E21.447Vertical transistor, e.g., tecnetrons (EPO) E21.448With heterojunction gate (EPO) E21.449Active layer is Group III-V compound (EPO) E21.451Active layer being Group III-V compound (EPO) E21.452Active layer being Group III-V compound (EPO) E21.453Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) E21.450Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) E21.461Using diffusion or decomposition of ecompound (EPO) E21.464Using liquid deposition (EPO) E21.465From molten solution of compound or alloy, e.g., liquid phase epitaxy (EPO) E21.465From molten solution of compound or alloy, e.g., liquid phase epitaxy (EPO) E21.466Diffusion of impurity material, e.g., dopant, electrode material, into or out of solid from or into gase out of solid from or into solid phase, e.g., doped oxide layer (EPO) E21.468Using diffusion into or out of solid from or into solid phase, e.g., doped oxide layer (EPO) E21.469Using diffusion into or out of solid from or into solid phase, e.g., doped oxide layer (EPO) E21.470Using diffusion into or out of solid from or into solid	E21.441	source or drain (EPO)Active layer is Group III-	E21.462	Using physical deposition, e.g., vacuum deposition,
E21.443Using self-aligned punch through stopper or threshold implant under gate region (EPO) E21.444Using dummy gate wherein at least part of final gate is self-aligned to dummy gate (EPO) E21.445With PN junction or heterojunction gate (EPO) E21.446With PN homojunction gate (EPO) E21.447Vertical transistor, e.g., tecnetrons (EPO) E21.448With heterojunction gate (EPO) E21.449Active layer is Group III-V compound (EPO) E21.451Active layer being Group III-V compound (EPO) E21.452Lateral single-gate transistors (EPO) E21.453Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) E21.453Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) E21.450Lateral single-gate transistors (EPO) E21.451Active layer being Group actions of solid from or into solid phase, e.g., alloy diffusion process (EPO) E21.453Active layer being Group actions of solid from or into solid phase, e.g., alloy diffusion process (EPO) E21.451Active layer being Group actions of solid from or into solid phase, e.g., alloy diffusion process (EPO) E21.452Lateral single-gate transistors (EPO) E21.453Active layer being Group action (EPO) E21.454Active layer being Group action (EPO) E21.455Active layer being Group actions of solid from or into solid phase, e.g., alloy diffusion process (EPO) E21.455Active layer, e.g., dummy-gate process (EPO) E21.456Using diffusion into or out of solid from or into solid phase, e.g., alloy diffusion process (EPO) E21.467Using diffusion into or out of solid from or into solid phase, e.g., alloy diffusion process (EPO) E21.469Using diffusion into or out of solid from or into solid phase, e.g., alloy diffusion process (EPO) E21.470Active layer, e.g., dummy-gate process (EPO)	E21.442	With gate at side of	E21.463	Using reduction or
E21.444Using dummy gate wherein at least part of final gate is self-aligned to dummy gate (EPO) E21.445With PN junction or heterojunction gate (EPO) E21.446With PN homojunction gate (EPO) E21.447Vertical transistor, e.g., tecnetrons (EPO) E21.448With heterojunction gate (EPO) E21.449With heterojunction gate (EPO) E21.451Active layer is Group III-V compound (EPO) E21.452Lateral single-gate transistors (EPO) E21.453Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) E21.451Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) E21.452Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) E21.453Process defend to dummy gate wherein at least part of final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) E21.454Using liquid deposition (EPO) E21.465From molten solution of compound or alloy, e.g., liquid phase epitaxy (EPO) E21.466Diffusion of impurity material, e.g., dopant, electrode material, into or out of semiconductor body, or between semiconductor regions (EPO) E21.467Using diffusion into or out of solid from or into solid phase, e.g., doped oxide layer (EPO) E21.468Using diffusion into or out of solid from or into solid phase, e.g., alloy diffusion process (EPO) E21.475Valloying of impurity material, e.g., dopant, electrode material, with semiconductor body (EPO)	E21.443	Using self-aligned punch through stopper or threshold		compound yielding solid condensate, i.e., chemical
at least part of final gate is self-aligned to dummy gate (EPO) E21.445With PN junction or heterojunction gate (EPO) E21.446With PN homojunction gate (EPO) E21.447Vertical transistor, e.g., tecnetrons (EPO) E21.448With heterojunction gate (EPO) E21.449Active layer is Group III-V compound (EPO) E21.451Active layer being Group III-V compound (EPO) E21.452Lateral single-gate transistors (EPO) E21.453Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) E21.45Process (EPO) E21.465From molten solution of compound or alloy, e.g., liquid phase epitaxy (EPO) E21.466Diffusion of impurity material, e.g., dopant, electrode material, into or out of semiconductor body, or between semiconductor regions (EPO) E21.467Using diffusion into or out of solid from or into gaseous phase (EPO) E21.468Using diffusion into or out of solid from or into solid phase, e.g., doped oxide layer (EPO) E21.469Using diffusion into or out of solid from or into liquid phase, e.g., alloy diffusion process (EPO) E21.47Lateral single-gate transistors (EPO) E21.48Valide phase epitaxy (EPO) E21.46Diffusion of impurity material, e.g., dopant, electrode material, e.g., dopan	TO1 444	(EPO)	E21.464	Using liquid deposition
E21.445With PN junction or heterojunction gate (EPO) E21.446With PN homojunction gate (EPO) E21.447Vertical transistor, e.g., tecnetrons (EPO) E21.448With heterojunction gate (EPO) E21.449Active layer is Group III-V compound (EPO) E21.45With Schottky gate, e.g., MESFET (EPO) E21.451Active layer being Group III-V compound (EPO) E21.452Lateral single-gate transistors (EPO) E21.453Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) E21.45With Schottky gate, e.g., dopant, electrode material, into or out of semiconductor body, or between semiconductor regions (EPO) E21.467Using diffusion into or out of solid from or into solid phase, e.g., doped oxide layer (EPO) E21.469Using diffusion into or out of solid from or into liquid phase, e.g., alloy diffusion process (EPO) E21.47Valloying of impurity material, e.g., dopant, electrode material, with semiconductor body (EPO)	E21.444	at least part of final gate is self-aligned to dummy gate	E21.465	From molten solution of compound or alloy, e.g.,
E21.446With PN homojunction gate (EPO) E21.447Vertical transistor, e.g., tecnetrons (EPO) E21.448With heterojunction gate (EPO) E21.449Active layer is Group III- V compound (EPO) E21.45With Schottky gate, e.g., MESFET (EPO) E21.451Active layer being Group III-V compound (EPO) E21.452Lateral single-gate transistors (EPO) E21.453Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) E21.47Lateral, into or out of semiconductor regions (EPO) E21.467Using diffusion into or out of solid from or into solid phase, e.g., doped oxide layer (EPO) E21.469Using diffusion into or out of solid from or into liquid phase, e.g., alloy diffusion process (EPO) E21.47Alloying of impurity material, e.g., dopant, electrode material, with semiconductor body (EPO)	E21.445	With PN junction or	E21.466	Diffusion of impurity
e.g., tecnetrons (EPO) E21.448With heterojunction gate (EPO) E21.449Active layer is Group III- V compound (EPO) E21.45With Schottky gate, e.g., MESFET (EPO) E21.451Active layer being Group III-V compound (EPO) E21.452Lateral single-gate transistors (EPO) E21.453Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) E21.45Process (EPO) E21.45Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) E21.45Sing diffusion into or out of solid from or into solid phase, e.g., doped oxide layer (EPO) E21.469Using diffusion into or out of solid from or into liquid phase, e.g., alloy diffusion process (EPO) E21.47Alloying of impurity material, e.g., dopant, electrode material, with semiconductor body (EPO)	E21.446	With PN homojunction gate		electrode material, into or
(EPO) E21.449Active layer is Group III- V compound (EPO) E21.45With Schottky gate, e.g., MESFET (EPO) E21.451Active layer being Group III-V compound (EPO) E21.452Lateral single-gate transistors (EPO) E21.453Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) of solid from or into gaseous phase (EPO) E21.468Using diffusion into or out (EPO) E21.469Using diffusion into or out of solid from or into gaseous phase (EPO) E21.468Using diffusion into or out (EPO) E21.469Using diffusion into or out of solid from or into gaseous phase (EPO) E21.468Using diffusion into or out (EPO) E21.469Using diffusion into or out of solid from or into solid phase, e.g., doped oxide layer (EPO) E21.450Using diffusion into or out of solid from or into gaseous phase (EPO) E21.468Using diffusion into or out of solid from or into solid phase, e.g., doped oxide layer (EPO) E21.469Using diffusion into or out of solid from or into solid phase, e.g., doped oxide layer (EPO) E21.469Using diffusion into or out of solid from or into solid phase, e.g., doped oxide layer (EPO) E21.469Using diffusion into or out of solid from or into solid phase, e.g., doped oxide layer (EPO) E21.469Using diffusion into or out of solid from or into solid phase, e.g., doped oxide layer (EPO) E21.469Using diffusion into or out of solid from or into solid phase, e.g., doped oxide layer (EPO) E21.469Using diffusion into or out of solid from or into solid phase, e.g., doped oxide layer (EPO) E21.469Using diffusion into or out of solid from or into solid	E21.447			· ·
V compound (EPO) E21.45With Schottky gate, e.g., MESFET (EPO) E21.451Active layer being Group III-V compound (EPO) E21.452Lateral single-gate transistors (EPO) E21.453Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) E21.468Using diffusion into or out of solid from or into liquid phase, e.g., alloy diffusion process (EPO) E21.47Alloying of impurity material, e.g., dopant, electrode material, with semiconductor body (EPO)	E21.448		E21.467	of solid from or into gaseous
MESFET (EPO) E21.451Active layer being Group III-V compound (EPO) E21.452Lateral single-gate transistors (EPO) E21.453Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) phase, e.g., doped oxide layer (EPO) E21.469Using diffusion into or out of solid from or into liquid phase, e.g., alloy diffusion process (EPO) E21.47Alloying of impurity material, e.g., dopant, electrode material, with semiconductor body (EPO)	E21.449		E21.468	Using diffusion into or out
III-V compound (EPO) E21.452Lateral single-gate transistors (EPO) E21.453Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) E21.459Using diffusion into or out of solid from or into liquid phase, e.g., alloy diffusion process (EPO) E21.470Using diffusion into or out of solid from or into liquid phase, e.g., alloy diffusion process (EPO) E21.469Using diffusion into or out of solid from or into liquid phase, e.g., alloy diffusion material, e.g., dopant, electrode material, with semiconductor body (EPO)	E21.45			phase, e.g., doped oxide layer
transistors (EPO) E21.453Process wherein final gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) phase, e.g., alloy diffusion process (EPO) E21.47Alloying of impurity material, e.g., dopant, electrode material, with semiconductor body (EPO)	E21.451		E21.469	Using diffusion into or out
gate is made after formation of source and drain regions in active layer, e.g., dummy-gate process (EPO) E21.47Alloying of impurity material, e.g., dopant, electrode material, with semiconductor body (EPO)	E21.452			phase, e.g., alloy diffusion
of source and drain regions in material, e.g., dopant, electrode material, with process (EPO) semiconductor body (EPO)	E21.453	Process wherein final	EQ1 47	
process (EPO) semiconductor body (EPO)		of source and drain regions in	E21.4/	material, e.g., dopant,
			E21.471	

E21.472With high-energy radiation (EPO)	E21.493Inorganic layer (EPO) E21.494Composed of oxide or
E21.473Producing ion implantation (EPO)	glassy oxide or oxide-based glass (EPO)
E21.474Using mask (EPO) E21.475Using electromagnetic radiation, e.g., laser radiation (EPO)	E21.495Deposition of noninsulating, e.g., conductive -, resistive -, layer on insulating layer
E21.476Manufacture of electrodes on semiconductor bodies using processes or apparatus other than epitaxial growth, e.g., coating, diffusion, or alloying, or radiation treatment (EPO)	(EPO) E21.496Post treatment of layer (EPO) E21.497Thermal treatment for modifying property of semiconductor body, e.g., annealing, sintering (EPO)
E21.477Deposition of conductive or insulating materials for electrode (EPO)	E21.498Application of electric current or fields, e.g., for electroforming (EPO)
E21.478From gas or vapor, e.g., condensation (EPO) E21.479From liquid, e.g.,	E21.499Assembling semiconductor devices, e.g., packaging, including mounting,
electrolytic deposition (EPO)	encapsulating, or treatment of
E21.48Involving application of pressure, e.g., thermo compression bonding (EPO)	packaged semiconductor (EPO) E21.5Mounting semiconductor bodies in container (EPO)
E21.481Including application of mechanical vibration, e.g., ultrasonic vibration (EPO)	E21.501Providing fillings in container, e.g., gas fillings (EPO)
E21.482Treatment of semiconductor body using process other than electromagnetic radiation	E21.502Encapsulation, e.g., encapsulation layer, coating (EPO)
(EPO) E21.483To change their surface- physical characteristics or shape, e.g., etching, polishing, cutting (EPO)	E21.503Encapsulation of active face of flip chip device, e.g., under filling or under encapsulation of flip-chip, encapsulation perform on chip
E21.484 Mechanical treatment, e.g., grinding, ultrasonic treatment (EPO)	or mounting substrate (EPO) E21.504Moulds (EPO) E21.505Insulative mounting
E21.485Chemical or electrical treatment, e.g., electrolytic	semiconductor device on support (EPO) E21.506Attaching or detaching leads
etching (EPO) E21.486Using mask (EPO)	or other conductive members,
E21.487To form insulating layer thereon, e.g., for masking or by using photolithographic	to be used for carrying current to or from device in operation (EPO)
techniques; post treatment of these layers (EPO) E21.488Using mask (EPO) E21.489Post treatment of insulating layer (EPO)	E21.507Formation of contacts to semiconductor by use of metal layers separated by insulating layers, e.g., self-aligned contacts to source/drain or
E21.49Etching layer (EPO) E21.491Doping layer (EPO) E21.492Organic layer, e.g., photoresist (EPO)	emitter/base (EPO) E21.508Forming solder bumps (EPO) E21.509Involving soldering or alloying process, e.g., soldering wires (EPO)

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E21.51	Mounting on metallic conductive member (EPO)	E21.525	Procedures, i.e., sequence of activities consisting of
E21.511	Mounting on insulating member provided with metallic leads, e.g., flip-chip		plurality of measurement and correction, marking or sorting steps (EPO)
	mounting, conductive die mounting (EPO)	E21.526	Connection or disconnection of subentities or redundant parts
	Right-up bonding (EPO)Mounting on semiconductor conductive member (EPO)		of device in response to measurement, e.g., wafer scale, memory devices (EPO)
E21.514	Involving use of conductive adhesive (EPO)	E21.527	Optical enhancement of defects or not directly visible
E21.515	<pre>Involving use of mechanical auxiliary part without use of alloying or soldering process, e.g., pressure contacts (EPO)</pre>		<pre>states, e.g., selective electrolytic deposition, bubbles in liquids, light emission, color change (EPO)</pre>
E21.516	<pre>Involving automation techniques using film carriers (EPO)</pre>	E21.528	Acting in response to ongoing measurement without interruption of processing,
E21.517	Involving use of electron or laser beam (EPO)		e.g., endpoint detection, in- situ thickness measurement
E21.518	Involving application of mechanical vibration, e.g.,	E21.529	<pre>(EPO)Measuring as part of manufacturing process (EPO)</pre>
E21.519	ultrasonic vibration (EPO)Involving application of pressure, e.g., thermo- compression bonding (EPO)	E21.53	<pre>For structural parameters, e.g., thickness, line width, refractive index, temperature,</pre>
E21.52	Devices having no potential- jump barrier or surface barrier (EPO)		<pre>warp, bond strength, defects, optical inspection, electrical measurement of structural</pre>
E21.521	.Testing or measuring during manufacture or treatment or		<pre>dimensions, metallurgic measurement of diffusions (EPO)</pre>
	reliability measurement, i.e., testing of parts followed by no processing which modifies parts as such (EPO)	E21.531	For electrical parameters, e.g., resistance, deep-levels, CV, diffusions by electrical means (EPO)
E21.522	Structural arrangement (EPO)	₽21 5 22	.Manufacture or treatment of
E21.523	Additional lead-in	EZI.JJZ	devices consisting of
	metallization on device, e.g.,		plurality of solid-state
	additional pads or lands, lines in scribe line,		components formed in or on
	sacrificed conductors,		common substrate or of parts
	sacrificed frames (EPO)		thereof; manufacture of
E21.524	Circuit for characterizing or		integrated circuit devices or
	monitoring manufacturing	₽ 21 533	of parts thereof (EPO)Of thick- or thin-film circuits
	process, e.g., whole test die,	EZI.JJJ	or parts thereof (EPO)
	wafer filled with test	E21.534	Of thick-film circuits or
	structures, onboard devices incorporated on each die,		parts thereof (EPO)
	process/product control	E21.535	<pre>Of thin-film circuits or parts thereof (EPO)</pre>
	monitors or PCM, devices in	E21 536	Manufacture of specific parts
	<pre>scribe-line/kerf, drop-in devices (EPO)</pre>		of devices (EPO)

E21.537	Making of localized buried regions, e.g., buried collector layer, internal connection, substrate contacts	E21.55	Trench shape altered by local oxidation of silicon process step, e.g., trench corner rounding by LOCOS (EPO)
	<pre>(EPO)Making of internal connections, substrate contacts (EPO)</pre>	E21.551	Introducing impurities in trench side or bottom walls, e.g., for forming channel stoppers or alter isolation behavior (EPO)
	<pre>For Group III-V compound semiconductor integrated circuits (EPO)</pre>	E21.552	Using local oxidation of silicon, e.g., LOCOS, SWAMI,
E21.54	Making of isolation regions between components (EPO)	E21.553	SILO (EPO)In region recessed from
E21.541	Between components manufactured in active substrate comprising SiC		<pre>surface, e.g., in recess, groove, tub or trench region (EPO)</pre>
E21.542	compound semiconductor (EPO)Between components manufactured in active substrate comprising Group	E21.554	Using auxiliary pillars in recessed region, e.g., to form LOCOS over extended areas (EPO)
F21 543	III-V compound semiconductor (EPO)Between components	E21.555	Recessed region having shape other than rectangular, e.g., rounded or oblique shape
EZ1.343	manufactured in active		(EPO)
	<pre>substrate comprising Group II- VI compound semiconductor (EPO)</pre>	E21.556	<pre>Introducing electrical inactive or active impurities in local oxidation region,</pre>
	<pre>PN junction isolation (EPO)Dielectric regions, e.g., EPIC dielectric isolation, LOCOS; trench refilling</pre>		<pre>e.g., to alter LOCOS oxide growth characteristics or for additional isolation purpose (EPO)</pre>
	techniques, SOI technology, use of channel stoppers (EPO)	E21.557	Introducing electrical active impurities in local
E21.546	Using trench refilling with dielectric materials (EPO)		oxidation region solely for forming channel stoppers (EPO)
	<pre>Dielectric material being obtained by full chemical transformation of nondielectric materials, such as polycrystalline silicon, metals (EPO)Concurrent filling of</pre>	E21.558	Introducing both types of electrical active impurities in local oxidation region solely for forming channel stoppers, e.g., for isolation of complementary doped regions (EPO)
121.510	plurality of trenches having different trench shape or dimension, e.g., rectangular	E21.559	With plurality of successive local oxidation steps (EPO)
F21 540	<pre>and V-shaped trenches, wide and narrow trenches, shallow and deep trenches (EPO)0f trenches having shape</pre>	E21.56	Dielectric isolation using EPIC technique, i.e., epitaxial passivated integrated circuit (EPO)
1121.J 1 7	other than rectangular or V shape, e.g., rounded corners, oblique or rounded trench	E21.561	Using semiconductor or insulator technology, i.e., SOI technology (EPO)
	walls (EPO)	E21.562	Using selective deposition of single crystal silicon, e.g., Selective Epitaxial Growth (SEG) (EPO)

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E21.563Using silicon implanted buried insulating layers, e.g., oxide layers, i.e., SIMOX technique (EPO)	E21.582Characterized by formation and post treatment of conductors, e.g., patterning (EPO)
E21.564SOI together with lateral isolation, e.g., using local	E21.583Planarization; smoothing (EPO)
oxidation of silicon, or	E21.584Barrier, adhesion or liner
<pre>dielectric or polycrystalline material refilled trench or</pre>	layer (EPO) E21.585Filling of holes, grooves,
<pre>air gap isolation regions, e.g., completely isolated</pre>	vias or trenches with conductive material (EPO)
semiconductor islands (EPO)	E21.586By selective deposition of
E21.565Using full isolation by porous oxide silicon, i.e., FIPOS technique (EPO)	<pre>conductive material in vias, e.g., selective chemical vapor deposition on semiconductor</pre>
E21.566Using lateral overgrowth	material, plating (EPO)
technique, i.e., ELO techniques (EPO)	E21.587By deposition over sacrificial masking layer,
E21.567Using bonding technique	e.g., lift-off (EPO)
(EPO)	E21.588Reflowing or applying
E21.568With separation/ delamination along ion	<pre>pressure to fill contact hole, e.g., to remove voids (EPO)</pre>
implanted layer, e.g., "Smart- cut", "Unibond" (EPO)	E21.589By forming conductive members before deposition of
E21.569Using silicon etch back	protective insulating
technique, e.g., BESOI, ELTRAN (EPO)	<pre>material, e.g., pillars, studs (EPO)</pre>
E21.57With separation/	E21.59Local interconnects; local
delamination along porous	pads (EPO)
delamination along porous layer (EPO) E21.571Using selective deposition of single crystal silicon,	<pre>pads (EPO) E21.591Modifying pattern or</pre>
delamination along porous layer (EPO) E21.571Using selective deposition of single crystal silicon, i.e., SEG technique (EPO)	<pre>pads (EPO) E21.591Modifying pattern or</pre>
delamination along porous layer (EPO) E21.571Using selective deposition of single crystal silicon, i.e., SEG technique (EPO) E21.572Polycrystalline semiconductor	<pre>pads (EPO) E21.591Modifying pattern or</pre>
delamination along porous layer (EPO) E21.571Using selective deposition of single crystal silicon, i.e., SEG technique (EPO)	<pre>pads (EPO) E21.591Modifying pattern or</pre>
delamination along porous layer (EPO) E21.571Using selective deposition of single crystal silicon, i.e., SEG technique (EPO) E21.572Polycrystalline semiconductor regions (EPO) E21.573Air gaps (EPO) E21.574Isolation by field effect	pads (EPO) E21.591Modifying pattern or conductivity of conductive members, e.g., formation of alloys, reduction of contact resistances (EPO) E21.592By altering solid-state characteristics of conductive members, e.g., fuses, in situ
delamination along porous layer (EPO) E21.571Using selective deposition of single crystal silicon, i.e., SEG technique (EPO) E21.572Polycrystalline semiconductor regions (EPO) E21.573Air gaps (EPO) E21.574Isolation by field effect (EPO)	pads (EPO) E21.591Modifying pattern or conductivity of conductive members, e.g., formation of alloys, reduction of contact resistances (EPO) E21.592By altering solid-state characteristics of conductive members, e.g., fuses, in situ oxidation, laser melting (EPO)
delamination along porous layer (EPO) E21.571Using selective deposition of single crystal silicon, i.e., SEG technique (EPO) E21.572Polycrystalline semiconductor regions (EPO) E21.573Air gaps (EPO) E21.574Isolation by field effect (EPO) E21.575Interconnections, comprising	pads (EPO) E21.591Modifying pattern or conductivity of conductive members, e.g., formation of alloys, reduction of contact resistances (EPO) E21.592By altering solid-state characteristics of conductive members, e.g., fuses, in situ oxidation, laser melting (EPO) E21.593By forming silicide of
delamination along porous layer (EPO) E21.571Using selective deposition of single crystal silicon, i.e., SEG technique (EPO) E21.572Polycrystalline semiconductor regions (EPO) E21.573Air gaps (EPO) E21.574Isolation by field effect (EPO)	pads (EPO) E21.591Modifying pattern or conductivity of conductive members, e.g., formation of alloys, reduction of contact resistances (EPO) E21.592By altering solid-state characteristics of conductive members, e.g., fuses, in situ oxidation, laser melting (EPO)
delamination along porous layer (EPO) E21.571Using selective deposition of single crystal silicon, i.e., SEG technique (EPO) E21.572Polycrystalline semiconductor regions (EPO) E21.573Air gaps (EPO) E21.574Isolation by field effect (EPO) E21.575Interconnections, comprising conductors and dielectrics, for carrying current between separate components within	pads (EPO) E21.591Modifying pattern or conductivity of conductive members, e.g., formation of alloys, reduction of contact resistances (EPO) E21.592By altering solid-state characteristics of conductive members, e.g., fuses, in situ oxidation, laser melting (EPO) E21.593By forming silicide of refractory metal (EPO) E21.594By using super-conducting material (EPO)
delamination along porous layer (EPO) E21.571Using selective deposition of single crystal silicon, i.e., SEG technique (EPO) E21.572Polycrystalline semiconductor regions (EPO) E21.573Air gaps (EPO) E21.574Isolation by field effect (EPO) E21.575Interconnections, comprising conductors and dielectrics, for carrying current between separate components within device (EPO)	pads (EPO) E21.591Modifying pattern or conductivity of conductive members, e.g., formation of alloys, reduction of contact resistances (EPO) E21.592By altering solid-state characteristics of conductive members, e.g., fuses, in situ oxidation, laser melting (EPO) E21.593By forming silicide of refractory metal (EPO) E21.594By using super-conducting material (EPO) E21.595Modifying pattern (EPO)
delamination along porous layer (EPO) E21.571Using selective deposition of single crystal silicon, i.e., SEG technique (EPO) E21.572Polycrystalline semiconductor regions (EPO) E21.573Air gaps (EPO) E21.574Isolation by field effect (EPO) E21.575Interconnections, comprising conductors and dielectrics, for carrying current between separate components within device (EPO) E21.576Characterized by formation and post treatment of	pads (EPO) E21.591Modifying pattern or conductivity of conductive members, e.g., formation of alloys, reduction of contact resistances (EPO) E21.592By altering solid-state characteristics of conductive members, e.g., fuses, in situ oxidation, laser melting (EPO) E21.593By forming silicide of refractory metal (EPO) E21.594By using super-conducting material (EPO) E21.595Modifying pattern (EPO) E21.596Using laser, e.g., laser cutting, laser direct writing,
delamination along porous layer (EPO) E21.571Using selective deposition of single crystal silicon, i.e., SEG technique (EPO) E21.572Polycrystalline semiconductor regions (EPO) E21.573Air gaps (EPO) E21.574Isolation by field effect (EPO) E21.575Interconnections, comprising conductors and dielectrics, for carrying current between separate components within device (EPO) E21.576Characterized by formation and post treatment of dielectrics, e.g., planarizing (EPO)	pads (EPO) E21.591Modifying pattern or conductivity of conductive members, e.g., formation of alloys, reduction of contact resistances (EPO) E21.592By altering solid-state characteristics of conductive members, e.g., fuses, in situ oxidation, laser melting (EPO) E21.593By forming silicide of refractory metal (EPO) E21.594By using super-conducting material (EPO) E21.595Modifying pattern (EPO) E21.596Using laser, e.g., laser
delamination along porous layer (EPO) E21.571Using selective deposition of single crystal silicon, i.e., SEG technique (EPO) E21.572Polycrystalline semiconductor regions (EPO) E21.573Air gaps (EPO) E21.574Isolation by field effect (EPO) E21.575Interconnections, comprising conductors and dielectrics, for carrying current between separate components within device (EPO) E21.576Characterized by formation and post treatment of dielectrics, e.g., planarizing (EPO) E21.577By forming via holes (EPO)	pads (EPO) E21.591Modifying pattern or conductivity of conductive members, e.g., formation of alloys, reduction of contact resistances (EPO) E21.592By altering solid-state characteristics of conductive members, e.g., fuses, in situ oxidation, laser melting (EPO) E21.593By forming silicide of refractory metal (EPO) E21.594By using super-conducting material (EPO) E21.595Modifying pattern (EPO) E21.596Using laser, e.g., laser cutting, laser direct writing, laser repair (EPO) E21.597Formed through semiconductor substrate (EPO)
delamination along porous layer (EPO) E21.571Using selective deposition of single crystal silicon, i.e., SEG technique (EPO) E21.572Polycrystalline semiconductor regions (EPO) E21.573Air gaps (EPO) E21.574Isolation by field effect (EPO) E21.575Interconnections, comprising conductors and dielectrics, for carrying current between separate components within device (EPO) E21.576Characterized by formation and post treatment of dielectrics, e.g., planarizing (EPO) E21.577By forming via holes (EPO) E21.578Tapered via holes (EPO)	pads (EPO) E21.591Modifying pattern or conductivity of conductive members, e.g., formation of alloys, reduction of contact resistances (EPO) E21.592By altering solid-state characteristics of conductive members, e.g., fuses, in situ oxidation, laser melting (EPO) E21.593By forming silicide of refractory metal (EPO) E21.594By using super-conducting material (EPO) E21.595Modifying pattern (EPO) E21.596Using laser, e.g., laser cutting, laser direct writing, laser repair (EPO) E21.597Formed through semiconductor substrate (EPO) E21.598Manufacture or treatment of
delamination along porous layer (EPO) E21.571Using selective deposition of single crystal silicon, i.e., SEG technique (EPO) E21.572Polycrystalline semiconductor regions (EPO) E21.573Air gaps (EPO) E21.574Isolation by field effect (EPO) E21.575Interconnections, comprising conductors and dielectrics, for carrying current between separate components within device (EPO) E21.576Characterized by formation and post treatment of dielectrics, e.g., planarizing (EPO) E21.577By forming via holes (EPO) E21.578Tapered via holes (EPO) E21.579For "dual damascene" type	pads (EPO) E21.591Modifying pattern or conductivity of conductive members, e.g., formation of alloys, reduction of contact resistances (EPO) E21.592By altering solid-state characteristics of conductive members, e.g., fuses, in situ oxidation, laser melting (EPO) E21.593By forming silicide of refractory metal (EPO) E21.594By using super-conducting material (EPO) E21.595Modifying pattern (EPO) E21.596Using laser, e.g., laser cutting, laser direct writing, laser repair (EPO) E21.597Formed through semiconductor substrate (EPO) E21.598Manufacture or treatment of devices consisting of
delamination along porous layer (EPO) E21.571Using selective deposition of single crystal silicon, i.e., SEG technique (EPO) E21.572Polycrystalline semiconductor regions (EPO) E21.573Air gaps (EPO) E21.574Isolation by field effect (EPO) E21.575Interconnections, comprising conductors and dielectrics, for carrying current between separate components within device (EPO) E21.576Characterized by formation and post treatment of dielectrics, e.g., planarizing (EPO) E21.577By forming via holes (EPO) E21.578Tapered via holes (EPO) E21.579For "dual damascene" type structures (EPO)	pads (EPO) E21.591Modifying pattern or conductivity of conductive members, e.g., formation of alloys, reduction of contact resistances (EPO) E21.592By altering solid-state characteristics of conductive members, e.g., fuses, in situ oxidation, laser melting (EPO) E21.593By forming silicide of refractory metal (EPO) E21.594By using super-conducting material (EPO) E21.595Modifying pattern (EPO) E21.596Modifying pattern (EPO) E21.597Formed through semiconductor substrate (EPO) E21.598Manufacture or treatment of devices consisting of plurality of solid-state
delamination along porous layer (EPO) E21.571Using selective deposition of single crystal silicon, i.e., SEG technique (EPO) E21.572Polycrystalline semiconductor regions (EPO) E21.573Air gaps (EPO) E21.574Isolation by field effect (EPO) E21.575Interconnections, comprising conductors and dielectrics, for carrying current between separate components within device (EPO) E21.576Characterized by formation and post treatment of dielectrics, e.g., planarizing (EPO) E21.577By forming via holes (EPO) E21.578Tapered via holes (EPO) E21.579For "dual damascene" type structures (EPO)	pads (EPO) E21.591Modifying pattern or conductivity of conductive members, e.g., formation of alloys, reduction of contact resistances (EPO) E21.592By altering solid-state characteristics of conductive members, e.g., fuses, in situ oxidation, laser melting (EPO) E21.593By forming silicide of refractory metal (EPO) E21.594By using super-conducting material (EPO) E21.595Modifying pattern (EPO) E21.596Using laser, e.g., laser cutting, laser direct writing, laser repair (EPO) E21.597Formed through semiconductor substrate (EPO) E21.598Manufacture or treatment of devices consisting of

E21.599With subsequent division of substrate into plural	E21.619With particular manufacturing method of source
<pre>individual devices (EPO) E21.6Involving separation of</pre>	or drain, e.g., specific S or D implants or silicided S or D structures or raised S or D structures (EPO)
E21.601Leaving reusable substrate, e.g., epitaxial lift-off process (EPO)	E21.62Manufacturing common source or drain regions between plurality of conductor-insulator-
E21.602 To produce devices each consisting of plurality of components, e.g., integrated	semiconductor structures (EPO) E21.621With particular
circuits (EPO) E21.603Substrate is semiconductor, using combination of	<pre>manufacturing method of gate conductor, e.g., particular materials, shapes (EPO)</pre>
semiconductor substrates, e.g., diamond, SiC, Si, Group	E21.622Silicided or salicided gate conductors (EPO)
<pre>III-V compound, and/or Group II-VI compound semiconductor substrates (EPO)</pre>	E21.623Gate conductors with different gate conductor materials or different gate
E21.604Substrate is semiconductor, using diamond technology (EPO)	<pre>conductor implants, e.g., dual gate structures (EPO)</pre>
E21.605Substrate is semiconductor, using SiC technology (EPO)	E21.624Gate conductors with different shapes, lengths or
E21.606Substrate being semiconductor, using silicon	dimensions (EPO) E21.625With particular
technology (EPO) E21.608Bipolar technology (EPO) E21.609Comprising combination of vertical and lateral	<pre>manufacturing method of gate insulating layer, e.g., different gate insulating layer thicknesses, particular</pre>
transistors (EPO) E21.61Comprising merged	gate insulator materials or particular gate insulator implants (EPO)
transistor logic or integrated injection logic (EPO)	E21.626With particular manufacturing method of gate
E21.611Complementary devices, e.g., complementary transistors (EPO)	sidewall spacers, e.g., double spacers, particular spacer material or shape (EPO)
E21.612Complementary vertical transistors (EPO)	E21.627Interconnection or wiring
E21.613Memory structures (EPO) E21.614Three-dimensional	or contact manufacturing related aspects (EPO)
integrated circuits stacked in different levels (EPO)	E21.628Isolation region manufacturing related aspects, e.g., to avoid interaction of
E21.615Field-effect technology (EPO)	isolation region with adjacent
E21.616MIS technology (EPO) E21.617Combination of charge coupled devices, i.e., CCD or BBD (EPO)	structure (EPO) E21.629With particular manufacturing method of vertical transistor structures, i.e., with channel
E21.618With particular manufacturing method of channel, e.g., channel implants, halo or pocket implants, or channel materials (EPO)	vertical to substrate surface (EPO)

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E21.63With particular	E21.642Isolation region
manufacturing method of wells	manufacturing related aspects,
or tubs, e.g., twin tubs, high	e.g., to avoid interaction of
energy well implants, buried	isolation region with adjacent
implanted layers for lateral	structure (EPO)
isolation (BILLI) (EPO)	E21.643With particular
E21.631Combination of	manufacturing method of
enhancement and depletion	vertical transistor
transistors (EPO)	structures, i.e., with channel
E21.632Complementary field-	vertical to substrate surface
effect transistors, e.g., CMOS	(EPO)
(EPO)	E21.644With particular
E21.633With particular	manufacturing method of wells
manufacturing method of	or tubs, e.g., twin tubs, high energy well implants, buried
channel, e.g., channel implants, halo or pocket	implanted layers for lateral
implants, or channel materials	isolation (BILLI) (EPO)
(EPO)	E21.645Memory structures (EPO)
E21.634With particular	E21.646Dynamic random access
manufacturing method of source	memory structures (DRAM) (EPO)
or drain, e.g., specific S or	E21.647Characterized by type of
D implants or silicided S or D	capacitor (EPO)
structures or raised S or D	E21.648Capacitor stacked over
structures (EPO)	transfer transis tor (EPO)
E21.635With particular	E21.649Making connection
manufacturing method of gate	between transistor and
<pre>conductor, e.g., particular materials, shapes (EPO)</pre>	capacitor, e.g., plug (EPO)
E21.636Silicided or salicided	E21.65Capacitor extending under transfer transistor area
gate conductors (EPO)	(EPO)
E21.637Gate conductors with	E21.651Capacitor in U- or V-
different gate conductor	shaped trench in substrate
materials or different gate	(EPO)
conductor implants, e.g., dual	E21.652In combination with
gate structures (EPO)	vertical transistor (EPO)
E21.638Gate conductors with	E21.653Making connection
different shapes, lengths or	between transistor and
dimensions (EPO) E21.639With particular	capacitor, e.g., buried strap
manufacturing method of gate	(EPO)
insulating layer, e.g.,	E21.654Characterized by type
different gate insulating	of transistor; manufacturing of transistor (EPO)
layer thicknesses, particular	E21.655Transistor in U- or V-
gate insulator materials or	shaped trench in substrate
particular gate insulator	(EPO)
implants (EPO)	E21.656
E21.64With particular	lines (EPO)
manufacturing method of gate	E21.657Making bit line (EPO)
sidewall spacers, e.g., double	E21.658Making bit line
spacers, particular spacer material or shape (EPO)	contact (EPO)
E21.641Interconnection or	E21.659Making word line (EPO)
wiring or contact	E21.66Simultaneous
manufacturing related aspects	fabrication of periphery and
(EPO)	memory cells (EPO) E21.661Static random access
	memory structures (SRAM) (EPO)
	memory structures (SRAM) (EPO)

E21.662	Read-only memory structures (ROM), i.e.,	E21.683	Simultaneous
	nonvolatile memory structures (EPO)		memory cells (EPO)Including one type
E21.663	nonvolatile memory structures		of peripheral FET (EPO)Control gate layer
E21.664	(EPO)With ferroelectric	E21.686	used for peripheral FET (EPO)Intergate
E21.665	capacitor (EPO)Magnetic nonvolatile		dielectric layer used for peripheral FET (EPO)
= 01 .ccc	memory structures, e.g., MRAM (EPO)	E21.687	Floating gate layer used for peripheral FET
	PROM (EPO)	TO1 600	(EPO)
	ROM only (EPO)With source and drain on same level, e.g., lateral	E21.088	Floating gate dielectric layer used for peripheral FET (EPO)
	channel (EPO)	E21.689	Including different
E21.669	Source or drain		types of peripheral FETs (EPO)
	contact programmed (EPO)	E21.69	With source and drain
	programmed (EPO)		on same level and with cell select transistor (EPO)
E21.671	Doping programmed,	E21.691	Simultaneous
E21 672	e.g., mask ROM (EPO)Entire channel		fabrication of periphery and memory cells (EPO)
121.072	doping programmed (EPO)	E21.692	
E21.673	Source or drain doping programmed (EPO)		on different levels, e.g., sloping channel (EPO)
E21.674	Gate programmed, e.g., different gate material		For vertical channel (EPO)
	or no gate (EPO)	E21.694	
E21.675		TO1 COE	control gate (EPO)
-04 656	<pre>programmed, e.g., different thickness (EPO)</pre>	E21.695	Combination of bipolar and field-effect technologies
E21.676		₽21 606	(EPO)Bipolar and MOS
	on different levels, e.g., vertical channel (EPO)		technologies (EPO)
E21.677		E21.697	Substrate is Group III-V
E01 (70	levels, e.g., 3D ROM (EPO)	E21 600	semiconductor (EPO)
E21.0/8	Simultaneous fabrication of periphery and		Substrate is Group II-VI semiconductor (EPO)
E01 670	memory cells (EPO)	E21.699	Substrate is semiconductor
E21.6/9			other than diamond, SiC, Si, Group III-V compound, or Group II-VI compound (EPO)
E21.68	Electrically	E21.7	Substrate is nonsemiconductor
	<pre>programmable (EPROM), i.e., floating gate memory</pre>		<pre>body, e.g., insulating body (EPO)</pre>
	structures (EPO)	E21.701	Substrate is sapphire, e.g.,
	With conductive layer as control gate (EPO)		silicon on sapphire structure (SOS) (EPO)
E21.682	With source and drain	E21.702	To produce devices, each
	on same level and without cell select transistor (EPO)		<pre>consisting of single circuit element (EPO)</pre>
		E21.703	Substrate is semiconductor body (EPO)

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E21.704	Substrate is nonsemiconductor body, e.g.,	917	PLURAL DOPANTS OF SAME CONDUCTIVITY TYPE IN SAME
E21.705	<pre>insulating body (EPO)Assembly of devices consisting of solid-state components formed in or on a common substrate; assembly of</pre>	918	REGION LIGHT EMITTING REGENERATIVE SWITCHING DEVICE (E.G., LIGHT EMITTING SCR) ARRAYS, CIRCUITRY, ETC.
	integrated circuit devices (EPO)	919	ELEMENTS OF SIMILAR CONSTRUCTION CONNECTED IN SERIES OR PARALLEL TO AVERAGE OUT
CROSS-R	EFERENCE ART COLLECTIONS		MANUFACTURING VARIATIONS IN CHARACTERISTICS
900	MOSFET TYPE GATE SIDEWALL INSULATING SPACER	920	CONDUCTOR LAYERS ON DIFFERENT LEVELS CONNECTED IN PARALLEL
901	MOSFET SUBSTRATE BIAS		(E.G., TO REDUCE RESISTANCE)
902	FET WITH METAL SOURCE REGION	921	RADIATION HARDENED SEMICONDUCTOR
903	FET CONFIGURATION ADAPTED FOR USE		DEVICE
J03	AS STATIC MEMORY CELL	922	WITH MEANS TO PREVENT INSPECTION
904			OF OR TAMPERING WITH AN
904	.WITH PASSIVE COMPONENTS, (e.g.,		INTEGRATED CIRCUIT (E.G.,
005	POLYSILICON RESISTORS)		"SMART CARD", ANTI-TAMPER)
905	PLURAL DRAM CELLS SHARE COMMON	923	WITH MEANS TO OPTIMIZE ELECTRICAL
006	CONTACT OR COMMON TRENCH	720	CONDUCTOR CURRENT CARRYING
906	DRAM WITH CAPACITOR ELECTRODES		CAPACITY (E.G., PARTICULAR
	USED FOR ACCESSING (E.G., BIT		CONDUCTOR ASPECT RATIO)
	LINE IS CAPACITOR PLATE)	924	WITH PASSIVE DEVICE (E.G.,
907	FOLDED BIT LINE DRAM	7 - 1	CAPACITOR), OR BATTERY, AS
	CONFIGURATION		INTEGRAL PART OF HOUSING OR
908	DRAM CONFIGURATION WITH		HOUSING ELEMENT (E.G., CAP)
	TRANSISTORS AND CAPACITORS OF	925	BRIDGE RECTIFIER MODULE
	PAIRS OF CELLS ALONG A	926	ELONGATED LEAD EXTENDING AXIALLY
	STRAIGHT LINE BETWEEN ADJACENT	J20	THROUGH ANOTHER ELONGATED LEAD
	BIT LINES	927	DIFFERENT DOPING LEVELS IN
909	MACROCELL ARRAYS (E.G., GATE	221	DIFFERENT PARTS OF PN JUNCTION
	ARRAYS WITH VARIABLE SIZE OR		TO PRODUCE SHAPED DEPLETION
	CONFIGURATION OF CELLS)		LAYER
910	DIODE ARRAYS (E.G., DIODE READ-	928	WITH SHORTED PN OR SCHOTTKY
	ONLY MEMORY ARRAY)	220	JUNCTION OTHER THAN EMITTER
911	LIGHT SENSITIVE ARRAY ADAPTED TO		JUNCTION
	BE SCANNED BY ELECTRON BEAM	929	PN JUNCTION ISOLATED INTEGRATED
	(E.G., VIDICON DEVICE)	727	CIRCUIT WITH ISOLATION WALLS
912	CHARGE TRANSFER DEVICE USING BOTH		HAVING MINIMUM DOPANT
	ELECTRON AND HOLE SIGNAL		CONCENTRATION AT INTERMEDIATE
	CARRIERS		DEPTH IN EPITAXIAL LAYER
913	WITH MEANS TO ABSORB OR LOCALIZE		(E.G., DIFFUSED FROM BOTH
	UNWANTED IMPURITIES OR DEFECTS		SURFACES OF EPITAXIAL LAYER)
	FROM SEMICONDUCTORS (E.G.,	930	THERMOELECTRIC (E.G., PELTIER
	HEAVY METAL GETTERING)		EFFECT) COOLING
914	POLYSILICON CONTAINING OXYGEN,		
	NITROGEN, OR CARBON (E.G.,		
0.4 =	SIPOS)		
915	WITH TITANIUM NITRIDE PORTION OR	₽ ∩D₽T <i>C</i> N	APT COLLECTIONS
	REGION	FOREIGN	ART COLLECTIONS
916	NARROW BAND GAP SEMICONDUCTOR		GLAGG DELAMED BODESCH DOGGETTE
	MATERIAL (>>1EV)	FOR UUU	CLASS-RELATED FOREIGN DOCUMENTS

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